SYNCOM

ECE Dept. NEWS LETTER

VOICE OF ELECTRONIC AND COMMUNICATION ENGINEERING

July 2019 Vol.4 Issue 07

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VISION, MISSION &PEO'S

Vision

Developing highly Qualitative, Technically Competent and Socially Responsible Engineers.

Mission

To provide quality education in the domain of Electronics and Communication Engineering through

- Enriched curriculum for addressing the needs of Industry.
- Effective teaching learning processes through congenial environment.
- Gaining contemporary knowledge through research, development, curricular, co and extra-curricular.

ECE Program Educational Objectives

Graduates of Electronics & Communication EngineeringShall

PEO1: Develop a strong background in basic science and mathematics and ability to use these tools in their chosen fields of specialization.

PEO2: Have the ability to demonstrate technical competence in the fields of electronics and communication engineering and develop solutions to the problems.

PEO3: Attain professional competence through life-long learning such as advanced degrees, professional registration, and other professional activities.

PEO4: Function effectively in a multi-disciplinary environment and individually, within a global, societal, and environmental context.

PEO5: Take individual responsibility and to work as a part of a team towards the fulfillment of both individual and organizational goals.

The institute is a symbol of egalitarian outlook without discretions. KITS student activity council is organized exclusively by students with representatives from various disciplines stands for the advocacy of democracy and leadership opportunities provided by the institute. KITS student clubs enable all the students and staff mingle freely to express their views and share their talents and expertise. **KITS imparts Outcome Based Education (OBE)** which gives equal opportunities to teaching and learning curricular, co-curricular and extra-curricular activities

Faculty Development Program:

The ECE department faculty attended for A national level Summer Faculty Development program conducted by An Initiative of Ministry of Electronics & IT, Govt. of India from 08th July to 15th July on "VLSI Chip Design hands on using open source EDA".

About Summer Courses:

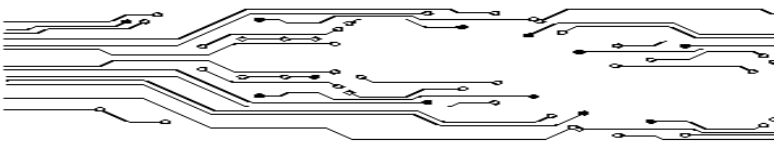
Faculty Development Programmes in core areas of Electronics and Information & Communication Technology (ICT) streams have been planned by academies for delivery during Summers (i.e., May – July 2019). All these summer courses will be offered through National Knowledge Network (NKN) based Video Conferencing, with lectures delivered by invited experts from IITs, NITs, IIITs and other premier institutes/industries. In addition, local course coordinators at respective academies /identified remote centres will take care of sessions on design orientation/activity linked problems/ assignments/ case studies and quiz test(s). All seven EICT Academies will host the participants simultaneously along with some select remote centres all over our country, through NKN-VC infrastructure. Candidates could attend the training programme at Academy locations or at identified remote centres as per the convenience.

Course Objectives:

This course is designed to provide an exposure to the fundamentals of VLSI chip designing. Participants will learn Floor Planning, placement and global routing. Hands-on training and practice sessions will help participants gain confidence on Analog and Mixed Signal Circuits, their simulation and implementation including sessions on chip designing using EDA Tools. The course will be useful for faculty of engineering and sciences who are interested in the learning VLSI chip designing.

The following Modules are covered in the FDP Program

- SoC Design (RISC-V SoC, which implements RISC-V IMC ISA
- Pre-layout timing analysis (Lab - OpenSTA) and Floorplanning
- Placement, Clock tree synthesis, Routing and SI
- Post-layout STA
- ECO
- Important aspects, particular to Analog/Mixed signal IC design



WORKSHOP

III year students participated in a workshop from 03rd July to 5th July on "LAB VIEW Applications" by VI Solutions,Bangalore .

LabVIEW is systems engineering software for applications that require test, measurement, and control with rapid access to hardware and data insights.

LabVIEW offers a graphical programming approach that helps you visualize every aspect of your application, including hardware configuration, measurement data, and debugging. This visualization makes it simple to integrate measurement hardware from any vendor, represent complex logic on the diagram, develop data analysis algorithms, and design custom engineering user interfaces.

Dataflow programming

The programming paradigm used in LabVIEW, sometimes called G, is based on data availability. If there is enough data available to a subVI or function, that subVI or function will execute. Execution flow is determined by the structure of a graphical block diagram (the LabVIEW-source code) on which the programmer connects different function-nodes by drawing wires. These wires propagate variables and any node can execute as soon as all its input data become available. Since this might be the case for multiple nodes simultaneously, LabVIEW can execute inherently in parallel.Multi-processing and multi-threading hardware is exploited automatically by the built-in scheduler, which multiplexes multiple OS threads over the nodes ready for execution.

Graphical programming

LabVIEW integrates the creation of user interfaces (termed front panels) into the development cycle. LabVIEW programs-subroutines are termed virtual instruments (VIs). Each VI has three components: a block diagram, a front panel, and a connector pane. The

last is used to represent the VI in the block diagrams of other, calling VIs. The front panel is built using controls and indicators. Controls are inputs: they allow a user to supply information to the VI. Indicators are outputs: they indicate, or display, the results based on the inputs given to the VI. The back panel, which is a block diagram, contains the graphical source code. All of the objects placed on the front panel will appear on the back panel as terminals. The back panel also contains structures and functions which perform operations on controls and supply data to indicators. The structures and functions are found on the Functions palette and can be placed on the back panel. Collectively controls, indicators, structures, and functions are referred to as nodes. Nodes are connected to one another using wires, e.g., two controls and an indicator can be wired to the addition function so that the indicator displays the sum of the two controls. Thus a virtual instrument can be run as either a program, with the front panel serving as a user interface, or, when dropped as a node onto the block diagram, the front panel defines the inputs and outputs for the node through the connector pane. This implies each VI can be easily tested before being embedded as a subroutine into a larger program.

The graphical approach also allows nonprogrammers to build programs by dragging and dropping virtual representations of lab equipment with which they are already familiar. The LabVIEW programming environment, with the included examples and documentation, makes it simple to create small applications. This is a benefit on one side, but there is also a certain danger of underestimating the expertise needed for high-quality G programming. For complex algorithms or large-scale code, it is important that a programmer possess an extensive knowledge of the special LabVIEW syntax and the topology of its memory management. The most advanced LabVIEW development systems offer the ability to build stand-alone applications.

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Student Activities'

The following III ECE students participated in **"DRONE AWARNESS WORKSHOP"** Organized by IEEE Student Branch (#STB11430) of JNTUK University College of Engineering, Narsaraopet in Association with Fopple technologies on 27th July 2019.

S.No	Roll.No	Name
1.	17JR1A04C5	POPURI LAVANYA
2.	17JR1A04D6	SHAIK AFFRIN
3.	17JR1A04D9	SIKHAKOLLI DURGA SRI SRAVYA
4.	17JR1A04E3	SUNKARA PRASANNA SHANMUKHI
5.	17JR1A04E6	TEJASWI ARIKA
6.	17JR1A04E9	UMA CHANDRIKA EVURI
7.	17JR1A04F0	VUDDANTI TRIVENI
8.	17JR1A04F1	YADLA NEERAJAKSHI
9.	17JR1A04F2	YAMPARALA RAMYA
10.	17JR1A04F3	YEKKALA TULASI
11.	17JR1A04F4	YERRAMALLI SYAMALA
12.	17JR1A04F5	NALLURI VENU GOPAL
13.	17JR1A04G0	PANGA KOMALVENKATSAI
14.	17JR1A04G1	P. BHARADWAJ
15.	17JR1A04G3	PREM CHAND TALLAPANENI
16.	17JR1A04G6	SHAIK ASIF PASHA
17.	17JR1A04G8	SHAIK KHADAR VALI
18.	17JR1A04G9	SHAIK MAHABOOB SUBHANI
19.	17JR1A04H0	SHAIK MASTAN VALI
20.	17JR1A04H1	SIDDABATTUNI HARINADH
21.	17JR1A04H2	SIVA KRISHNA VEMULA

Faculty Achievements:

Prof. K. MadhuSudhanRao, Attended for A national level Summer Faculty Development program conducted by An Initiative of Ministry of Electronics & IT, Govt. of India from 08th July to 15th July on "VLSI Chip Design hands on using open source EDA".

Dr.Ch.Aruna Bala published a paper on **"TEXT SENTIMENT ANALYSIS BASED ON CNNS AND SVM**" in *International Journal of Research - GRANTHAALAYAH*.Vol.7 (Iss.6): June 2019 , **ISSN- 2350-0530(O), ISSN- 2394-3629(P)**

Mr.Maduguri Sudhir Attended for A national level Summer Faculty Development program conducted by An Initiative of Ministry of Electronics & IT, Govt. of India from 08th July to 15th July on "VLSI Chip Design hands on using open source EDA".

Ms. P.Jwalitha, Assitant Proffesor published a paper on **"TEXT SENTIMENT ANALYSIS BASED ON CNNS AND SVM**" in *International Journal of Research - GRANTHAALAYAH*.Vol.7 (Iss.6): June 2019 ,**ISSN- 2350-0530(O), ISSN- 2394-3629(P).**

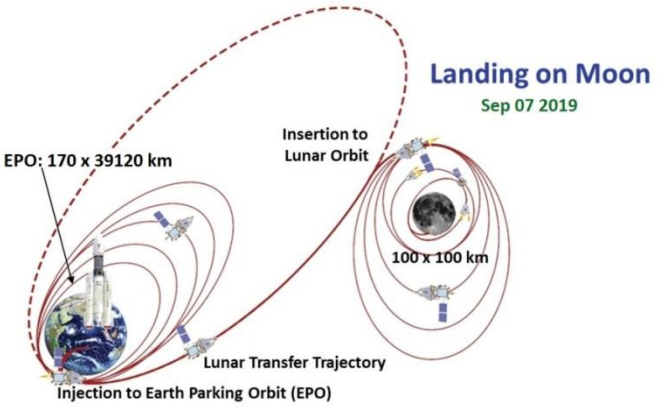
Ms.NuthalapatiSoniya Attended for A national level Summer Faculty Development program conducted by An Initiative of Ministry of Electronics & IT, Govt. of India from 08th July to 15th July on "VLSI Chip Design hands on using open source EDA".

Mr.MangipudiVenu Attended for A national level Summer Faculty Development program conducted by An Initiative of Ministry of Electronics & IT, Govt. of India from 08th July to 15th July on "VLSI Chip Design hands on using open source EDA".

Mr.K.Mallikarjuna Attended for A national level Summer Faculty Development program conducted by An Initiative of Ministry of Electronics & IT, Govt. of India from 08th July to 15th July on "VLSI Chip Design hands on using open source EDA".

Chandrayaan-02

Chandrayaan-2 is India's second lunar exploration mission after Chandrayaan-1 Developed by the Indian Space Research Organisation (ISRO), the mission was launched from the second launch pad at SatishDhawan Space Centreon 22 July 2019 at 2.43 PM IST (09:13 UTC) to the Moon by a Geosynchronous Satellite Launch Vehicle Mark III(GSLV Mk III). The planned orbit has a perigee of 170 km and an apogee of 45475 km. It consists of a lunar orbiter, a lander, and a lunar rover named *Pragyan*, all developed in India The main scientific objective is to map the location and abundance of lunar water.The primary objectives of Chandrayaan-2 are to demonstrate the ability to soft-land on the lunar surface and operate a robotic rover on the surface. Scientific goals include studies of lunar topography, mineralogy, elemental abundance, the lunar exosphere, and signatures of hydroxyl and water ice. The orbiter will map the lunar surface and help to prepare 3D maps of it. The onboard radar will also map the surface while studying the water ice in the south polar region and thickness of the lunar regolith on the surface.



Launcher:

The GSLV Mk-III is India's most powerful launcher to date, and has been completely designed and fabricated from within the country.

Orbiter:

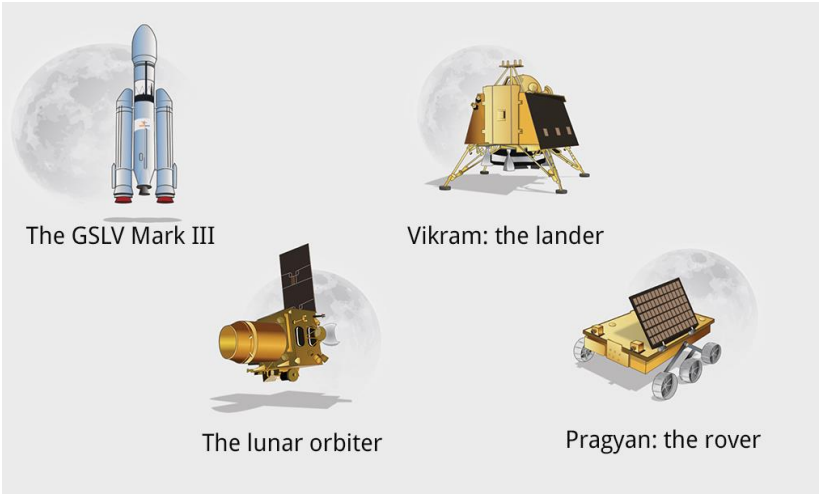
The Orbiter will observe the lunar surface and relay communication between Earth and Chandrayaan-2's lander Vikram.

Lander:

Lander Vikram is designed to execute India's first soft landing on the lunar surface.

Rover:

Rover Pragyan is a 6-wheeled, artificial intelligence-powered vehicle which translates to 'wisdom' in Sanskrit.



Team

The list below lists most instrumental scientists and engineers who were key to the development of Chandrayaan-2 project

- MuthayyaVanitha – Project Director, Chandrayaan-2
- RituKaridhal – Mission Director, Chandrayaan-2
- Chandrakanta Kumar – Deputy Project Director, Chandrayaan-2
- MylswamyAnnadurai – Project Director, Chandrayan-2

By/- Mr.G.Saketh
(IV ECE-A)

ULTRASONIC NAVIGATION SYSTEM FOR BLIND PEOPLE

This project is built to aid the blind so that they may walk easily in urban areas and avoid obstacles using special detection sensors. This system uses a microcontroller coupled with an output buzzer to alert the concerned. The system is fitted with ultrasonic sensors. The system guides and alerts the blind person of walking route and also alerts others about person at night through led's fitted with it .

The ultrasonic sensors fitted with the system provides obstacle data to the blind person so that he/she may avoid them . The LDR circuit coupled with LED lets other people and vehicles aware about the blind person in the dark. A microcontroller does all the work of detecting ultrasonic signals and sending back respectively messages to the blind person. Thus the system provides complete guidance and protection to a blind person under various circumstances.

By
Ms.Ch.Naveena (II ECE-A)

RISING TO THE ACCELERATION CHALLENGE

Artificial Intelligence (AI) and deep learning is the future of computing. Intelligent machines that understand the world as humans do, interpret our languages and learn from data will habitually be used to

resolve problems too complex for the human brain.

But progress in AI is being blocked by the simple lack of computing power. While scientists are building advanced algorithms, they do not yet have the hardware necessary to train machines on these algorithms nor for machines to execute the algorithms and apply their learning to new data. Although DeepMind's AlphaGo algorithm famously outsmarted the world's best Go player last year, it reportedly required 1202 CPUs and 176 GPUs (or in fact, Google's own TPUs) to do so – not exactly practical.

New solutions to hardware acceleration are required, so what is it about AI that requires a new approach to computing power and what are the possible options?

Basic forms of AI can function on traditional processors; for instance, IBM's Watson runs on a combination of power processors, GPUs and CPUs. Although Watson is often held up as the pinnacle of AI development, its functionality is limited to finding patterns and insights hidden in data. IBM is already looking to far more powerful processors to provide answers to questions where there is insufficient data to find patterns and the number of potential permutations is too vast to be processed by classical computers.

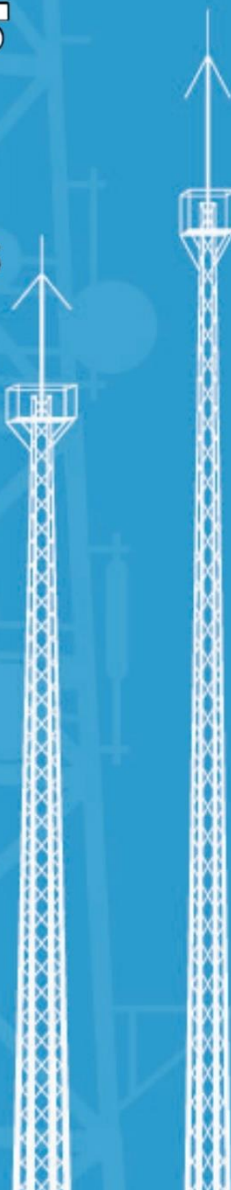
Deep learning is a new software model that requires a different type of computer platform. In deep neural networks, algorithms learn from data and examples, but effectively write their own software. This means software-neurons and connections must be trained in parallel, rather than sequentially.

Advances in CPUs have slowed and the marginal gains being delivered will not be sufficient to run deep neural networks effectively. A processing model is needed that can execute programmer-coded commands and the parallel training of deep neural networks.
Three approaches have emerged to meet the hardware acceleration challenge- Graphics processing, Tensor processing unit and FPGA

By
Mr. T.Bala Krishna
Assistant Professor

THE ART OF COMMUNICATION IS THE LANGUAGE OF LEADERSHIP....

- James Humes



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Department of Electronics and Communication Engineering