Code No: R1631043 **R16** SET - 1

III B. Tech I Semester Regular Examinations, October/November - 2018

DIGITAL IC APPLICATIONS

(Common to Electronics Communication Engineering and Electronics Instrumentation Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1.	a)	What are the advantages and disadvantages of CMOS technology?	[2M]
	b)	Give the program structure.	[2M]
	c)	What is the difference between if and case statement.	[2M]
	d)	Write a VHDL program for 4x1 multiplexer.	[3M]
	e)	What is the difference between Ring Counter and Twisted ring counter?	[3M]
	f)	Explain the significance of State Reduction.	[2M]

PART -B

2.	a)	Explain the terms i) DC noise margin ii) Fan-out with reference to TTL gate.	[7M]
	b)	Design CMOS transistor circuit for 3-input AND gate. With the help of function Tables explain the operation of the circuit diagram.	[7M]
3.	a)	Explain the structure of various LOOP statements in VHDL with examples.	[7M]
	b)	Explain the difference in program structure of VHDL and any other procedural language. Give an example.	[7M]
4.	a)	Design a 2 to 4 decoder circuit. Give its entity declaration behavioural model. Also draw the waveform giving relation between its inputs and outputs.	[7M]
	b)	Explain about variable assignment statement, signal assignment statement, wait statement.	[7M]
5.	a)	Design a 24-bit comparator circuit using 74×682 ICs and explain the functionality of the circuit. Also implement VHDL source code in data flow style.	[7M]
	b)	Design and implement counter using VHDL which counts up to 9 and down counts again from 9 to 0.	[7M]
6.	a)	Design a conversion circuit to convert a D flip-flop to J-K flip-flop. Write data-flow style VHDL program.	[7M]
	b)	Draw the circuit of a bidirectional shift register with parallel loading using 2 to 4 line decoder and D-flip-flops.	[7M]
7.	a)	What is meant by finite state machine? What are the capabilities and limitations of finite state machine?	[7M]
	b)	Write short notes on the following with suitable examples. i)State diagram ii)State table iii)state assignment	[7M]

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Code No: R1631043 **R16** SET - 2

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PART –A

1.	a)	Give the logic levels of CMOS and TTL families.	[2M]
	b)	What is Enumeration data type in VHDL? Give examples.	[2M]
	c)	Define and explain Loop statement.	[2M]
	d)	Write a VHDL program for 1 x 4 demultiplexer.	[3M]
	e)	Distinguish between Synchronous Counters and Asynchronous Counters.	[3M]
	f)	Define the terms State diagram and state table.	[2M]

PART -B

2.	a)	Draw the dynamic electrical behaviour of CMOS inverter and explain.	[7M]
	b)	Explain the differences between TTL, ECL & CMOS logic family.	[7M]
3.	a)	Discuss the binding? Discuss the binding between entity and components.	[7M]
	b)	Write a process based VHDL program for the prime-number detector of 4-bit input and explain the flow using logic circuit.	[7M]
4.	a)	Discuss Inertial Delay Model?	[7M]
	b)	Explain the concept of internal logic synthesizer and also draw the schematic.	[7M]
5.	a)	With the help of logic diagram explain 74×157 multiplexer. Write the data flow Style VHDL program for this IC?	[7M]
	b)	Explain about Comparator and design a 16-bit comparator using 74×85 IC's. Write VHDL program.	[7M]
6.	a)	Explain how a JK- flip-flop can be constructed using a T- flip-flop.	[7M]
	b)	Write down truth table, VHDL Code for the 4 bit register with parallel load. Also draw the circuit and output waveform.	[7M]
7.	a)	Explain the minimization of completely specified sequential machines.	[7M]
	b)	Convert the following melay machine into a corresponding Moore machine.	[7M]

P.S	NS,X=0	Z, X=1
A	B,0	E,0
B	E,0	D,0
C	D,1	A,0
D	C,1	E,0

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Code No: R1631043 **R16** SET - 3

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Time: 3 hours Max. Marks: 70

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2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1.	a)	Give the logic levels and noise margins of TTL families.	[2M]
	b)	Write a VHDL program for 2x4 Decoder.	[2M]
	c)	Define and explain Next statement.	[2M]
	d)	Explain about Barrel Shifter.	[3M]
	e)	List the various IC versions of shift registers.	[3M]
	f)	What is One hot encoding?	[2M]

PART -B

2.	a)	Explain the effect of floating inputs on CMOS gate.	[7M]
	b)	Draw the circuit diagram of basic TTL NAND gate and explain the three parts with the help of functional operation.	[7M]
3.	a)	Explain about dataflow design elements of VHDL.	[7M]
	b)	Write a VHDL program for comparing 8 bit unsigned integers.	[7M]
4.	a)	With examples explain the sequential assignment statements.	[7M]
	b)	Discuss Transport Delay Model.	[7M]
5.	a)	Draw the circuit of a 4-bit ripple carry adder circuit and explain how it is different from look-a-head carry circuit. Give the equation for C_1 to C_4 for a look-ahead carry adder circuit.	[7M]
	b)	Design a 4 to 16 decoder using two 74×138 decoders.	[7M]
6.	a)	Write down the VHDL code of S-R flip flop.	[7M]
	b)	Give a VHDL code for a 4-bit up counter with enable and clear inputs.	[7M]
7.	a)	Draw the logic diagram of Melay model & explore its operation with examples.	[7M]
	b)	Write down the VHDL code for the serial adder.	[7M]

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Code No: R1631043 **R16** SET - 4

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2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1. a) Explain the term Transition time with respect to CMOS logic. [2M]
   b) What are the operators available in VHDL? [2M]
   c) Define and explain assertion statement. [2M]
   d) Define three state devices. [3M]
   e) Write short note on Universal Shift Registers.. [3M]
   f) Distinguish between Mealy and Moore Machines. [2M]

PART -B

2. a) Design a CMOS transistor circuit for 3-input AND gate. With the help of function table explain the circuit. [7M]
   b) What is interfacing? Explain interfacing between low voltage TTL and low voltage CMOS logic. [7M]

3. a) Explain about the following i) Packages with syntax ii) Libraries with syntax. [7M]
   b) What is the Significance of time dimension in VHDL? Explain its function. [7M]

4. a) Explain about Inside of a logic synthesizer and Give its schematic. [7M]
   b) Discuss about Signal Drivers. [7M]

5. a) Write a VHDL code for 4-bit Look ahead carry generator. [7M]
   b) Implement the 32 input to 5 output priority encoder using four 74LS148 & gates. [7M]

6. a) Write down truth table, VHDL Code for the J-K flip flop using behavioural Modelling. [7M]
   b) Draw the circuit of MOD 16 Down ripple counter with D-flip-flops and explain its operation. [7M]

7. a) Draw the logic diagram of Moore model & explore its operation with examples. [7M]
   b) Explain the minimization procedure for determining the set of equivalent state of a specified machine M. [7M]

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