KKR&KSR Institute of Technology and Sciences
Vinjanampadu, Guntur, Andhra Pradesh-522017

Approved by AICTE, New Delhi and Permanent Affiliation from JNTUK, Kakinada
Accredited with "A" Grade by NAAC & NBA Accreditation Status for 4 UG (CSE, ECE, EEE, ME) Programs

A National Level Winter Faculty Development Programme
On VLSI Chip Design Hands-On Using Open Source EDA
(16th December 2019 to 20th December 2019)
By
Electronics & IT Academy, IIT Guwahati, Government of India

About E&IC Academy:

Department of Electronics and Information Technology (DeitY), Ministry of Communication and Information Technology (MCIT), Government of India (GoI) has set up an Electronics and ICT (E&ICT) Academy at IIT Guwahati along with four other such Academies. These Academies are being set up for faculty/mentor development and up gradation to improve the employability of graduates/diploma holders, in general, including those in Electronics and ICT streams, through the collaboration of State Governments with the financial assistance from the Central Government. These Academies are also entrusted to work towards creating a pool of skilled human resource in emerging areas in consonance with the Digital India and Electronic Design and Manufacturing (ESDM) initiatives of Government of India (GoI). The Academy at IIT Guwahati has been given the mandate to cover the North-East region. As per the mandate given by DeitY, each Electronics & ICT academy (E&ICT Academy) has to conduct various courses with Academic Partners and Industry Partners to train manpower in the area of emerging technologies and to impart knowledge in academic driven courses to increase employability.

Activities of the Academies

- Domain based training on use of ICT tools and techniques for non-engineering streams
- Faculty development Programmes
- Training and consultancy services for industry
- Curriculum development for industry
- Continuing Education programme for students / working professionals
- Design, Develop and Deliver specialized modules for specific research areas
- Providing advice and support for technical incubation and entrepreneurial activities

About Winter Courses

Faculty Development Programmes in core areas of Electronics and Information & Communication Technology (ICT) streams have been planned by academies for delivery during winters (i.e., Dec'19 – Jan'20). All these winter courses will be offered through National Knowledge Network (NKN) based Video Conferencing, with lectures delivered by invited experts from IITs, NITs, IIITs and other premier institutes/industries. In addition, local course coordinators at respective academies /identified remote centers will take care of sessions on design orientation/activity linked problems/ assignments/ case studies and quiz test(s). All EICT Academies will host the participants simultaneously along with some select remote centers all over our country, through NKN-VC infrastructure. Candidates could attend the training programme at Academy locations or at identified remote centers as per the convenience.

Contact Details

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1. **Objectives of the Event:**

VLSI Chip Design Hands on using open source EDA assumes importance from the point of view of wide spread use of digital signal processors design using VLSI for number of applications in various fields. This FDP aims to provide a broad coverage of techniques for designing efficient VLSI Chips. It Emphasis on the architectural research, design and optimization of VLSI systems. Faculty members will be able to teach and guide student's projects well both at B.Tech and at M.Tech level in this area. Also this FDP will enable them to take up or carry on research work in this area.

2. **Venue of the Event:**

The event is organized in **ECAD LAB** of KKR & KSR Institute of Technology and Sciences, Vinjanampadu, Guntur, Andhra Pradesh.

3. **Date & Time of the Event:** This is organized from 16th December 2019 to 20th December 2019
4. **No. of students participated:** Nil
5. **No. of faculties participated: 49**
6. **Event photographs.**

7. Benefits in terms of learning/Skill/Knowledge obtained.

The key benefits of the FDP is to assist faculty, who are in getting a broader view regarding the domain of VLSI design and familiarizing them with advanced research areas in VLSI systems. Faculty stands to benefit immensely from this opportunity to meet the experts in these fields. By participating in this FDP they will get a close look at the current trends in VLSI Systems and learn about the upcoming technological innovations. They will get a chance to ask questions regarding research opportunities and can seek advice from the best in the business. The FDP includes keynote speeches by veteran speakers from the Industry and it also features panel discussions. On completion of this FDP, faculty will receive a certification. Participating in FDP shall give them a feel of the real world technological challenges and ease their transition into the industry. In addition, it shall provide them with a better understanding to select appropriate and relevant research work.

Key Benefits and Takeaways:

- An opportunity to meet technology leaders
- An opportunity to learn from the experts in the field of VLSI Systems
- Understand the latest technology trends in VLSI Systems
- Understand expert views on Research
- Get an opportunity to network with industry professional.

8. One Participant Feed Back:

I am K.Mallikarjuna Rao, working as an assistant professor in ECE department in KKR & KSR Institute of Technology and Sciences. I have attended the **A National Level Winter Faculty Development Programme on VLSI Chip Design Hands-On Using Open Source EDA.** First of all I want to thank my college management who provided such facility for all of us to learn and experience these Faculty development programs. In this regard my sincere thanks to AICTE-MHRD-IIC and E & ICT Academy IIT Guwahati, who have been conducting such type of events for the faculty nourishment. I attended the FDP from 16th December to 20th December 2019. I learn the following key concepts from the FDP conducted on **VLSI Chip Design Hands-On Using Open Source EDA**.

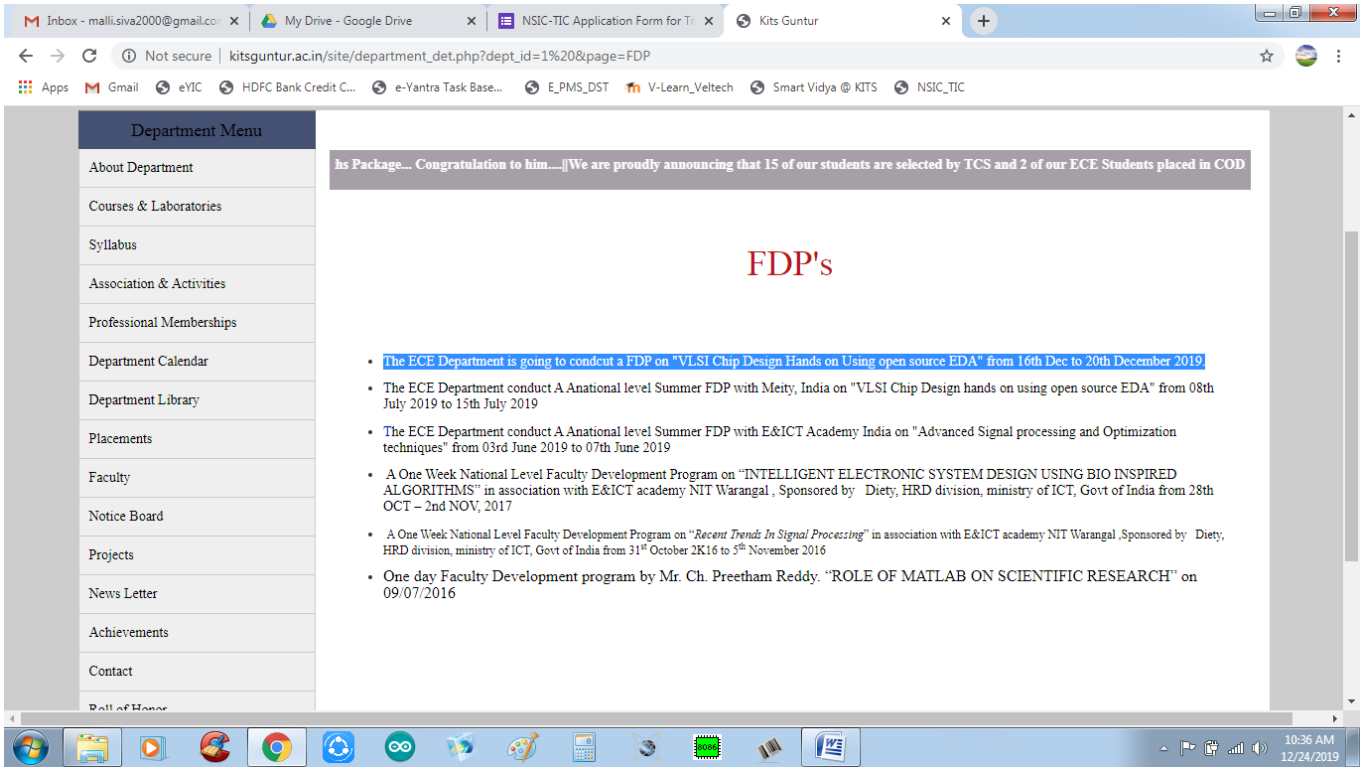
S.No.	Module Name	Topics
1.	Study various components of RISC-V microprocessor based SoC and review all components using MAGIC Layout tool	• Brief introduction RISC-V ISA • Overview of RISC-V based micro-processor and its related SoC • Overview of QFN48 package, pads, macros and memory in MAGIC • Idea of chip-planning, aspect ratio, utilization factor, power planning, decoupling capacitor, pads/memory and macro placement
2.	Study the importance of standard cell library and design & characterize one cell using MAGIC Layout tool and ngSPICE for SPICE simulations	• Pros and cons of good-bad floorplan • Introduction to lab to create floorplan for small design, which will be covered in detail on Day 4) • System-on-Chip (SoC) planning and design concepts overview • Physical design overview • Why Libraries are called the soul and heart of semi-conductor industry? • Standard cells library overview
3.	Pre-layout timing analysis of SoC using OpenSTA, chip planning using MAGIC and block-level placement/routing using qflow RTL2GDS opensource EDA toolchain	• Art of layout – Stick diagram + Euler's path using MAGIC • Characterization of important parameters using ngSPICE • Introduction to 16-Mask CMOS process and its significance to chip design flow • Logic synthesis and high fanout net synthesis interactive tutorial using Yosys opensource synthesis tool
4.	Hierarchical placement/routing using pads and blocks, and perform sign-off checks viz. LVS/DRC using Magic	• Introduction to static timing analysis and the related Industry standard reporting formats • Pre-layout timing analysis of a design using OpenSTA opensource STA tool, which includes setup timing analysis for reg2reg and IO • Introduction to clock tree synthesis (CTS) and its related checks viz. skew, latency, pulse-width, duty cycle • Placement/Routing/CTS of a design using qflow opensource RTL2GDS tool • Perform CTS quality and routing quality checks using OpenSTA
5.	Post-layout timing analysis using OpenSTA and engineering change order (ECO) using Tritonsizer	• Full chip integration using MAGIC for a design with blocks and pads. • Revise floorplan from Day 2 • Populate layout from library manager in MAGIC, select digital core block and additional pads • Arrange pads and create a pad-frame hierarchy • Project work using SiFive E31 RISC-V design blocks

9. **Promotion of the Event on the Social Media Website: (Link and Screenshot):**

https://www.facebook.com/photo.php?fbid=171723987558915&set=pcb.171724507558863&type=3&theater

10. **Promotion of the Event on the University/college Website :(Link and Screenshot)**

http://kitsguntur.ac.in/site/department_det.php?dept_id=1%20&page=FDP



11. 1- 2 minutes video of the event (Drive Link Only):

https://drive.google.com/open?id=1mVhvf552ZJMKbzgxGv7wzIXw_ZTOnimp

12. Expenditure Amount (If any): **RS.55,000**

13. Remarks: The FDP is organized smoothly with practical orientation.

14. Experiences and Output of the Session

Many Faculty members from inside and outside college are attended the FDP by **Electronics & IT Academy, IIT Guwahati, Government of India** from 16th December 2019 to 20th December 2019, conducted by KKR & KSR Institute of Technology and Sciences in association with MHRD-IIC.

Outcomes of the Session

Professors of Electronics & IT Academy, IIT Guwahati as resource persons FDP on "**VLSI Chip Design Hands-On Using Open Source EDA**" is organized. The session is Very useful and informative. **Eminent Professors of IIT Guwahati** explained very clear about basics and involved in practical examples. This FDP is very useful to understand current research trends and we want to learn more about this research. So it is better to extend this session. They explained the importance research in present scenario and government funding on innovative projects. Thank you very much to the management and MHRD-IIC for giving the opportunity.