KKR&KSR Institute of Technology and Sciences
Vinjanampadu, Guntur, Andhra Pradesh-522017

Approved by AICTE, New Delhi and Permanent Affiliation from JNTUK, Kakinada
Accredited with "A" Grade by NAAC & NBA Accreditation Status for 4 UG (CSE, ECE, EEE, ME) Programs

MHRD- IIC Report Format

FDP ON VLSI CHIP DESIGN HANDS ON USING OPEN SOURSE EDA TOOL

1. Objective of the Event:

   The objective of this event is to learn about Open Source EDA tool and to know how to write the code in the tool which will be useful in research purpose.

2. About the Program/Event:

   This programme was initiated by Ministry of Electronics & Information Technology (MeitY), Government of india under NKN Course series through online stream. The following topics have covered in both theoretical as well as practical through Open Source EDA tool.

   Faculty Development Programmes in core areas of Electronics and Information & Communication Technology (ICT) streams have been planned by academies for delivery during Summers (i.e., May – July 2019). All these summer courses will be offered through National Knowledge Network (NKN) based Video Conferencing, with lectures delivered by invited experts from IITs, NITs, IIITs and other premier institutes/industries. In addition, local course coordinators at respective academies /identified remote centres will take care of sessions on design orientation/activity linked problems/ assignments/ case studies and quiz test(s). All seven EICT Academies will host the participants simultaneously along with some select remote centres all over our country, through NKN-VC infrastructure. Candidates could attend the training programme at Academy locations or at identified remote centres as per the convenience.

3. Details of External Participants (If any):

S.NO	NAME	COLLEGE	MOBILE NO
1	J SAMBASIVA RAO	VIGNAN	9441816957
2	AV NAGESWARA RAO	NEC	9440664462

3	ZIA UR REHAMAN	KL UNIVERSITY	9440712707
4	T L K PRASANNA	TIRUMALA ENGINEERING COLLEGE	9398433270
5	V RAMA KRISHNA REDDY	NEC	9966221740
6	M SAILAJA	NEC	8686079929
7	N SRINIVASA RAO	VIGNAN	9573462080
8	CHARLES	MALINENI	9948942244
9	G SRINIVASA RAO	MALINENI	7660004132
10	K VIJAYAVARDAN	MALINENI	9581843414
11	VEERAYYA J	VIGNAN	9030263477
12	AZEEM	VIGNAN	9908122123
13	ANIL KUMAR	VIGNAN LARA	9885353468

4. Details of Resource Persons :

   Invited Talk 1 Dr. Anand Bulusu (IIT Roorkee)

   Interactive Lecture 1 Mr. Kunal P Ghosh (Director, VSD Corp. Pvt. Ltd.)

   Invited Talk 5 Mr. Uday Khambate (SCL Chandigarh)

   Invited Talk 4 Dr. H. S. Jatana (SCL Chandigarh)

   Invited Talk 2 Dr. Imon Mondal (IIT Kanpur)

   Invited Talk 3 Dr. Suhakumar Reddy (VEDA IIT Hyderabad)

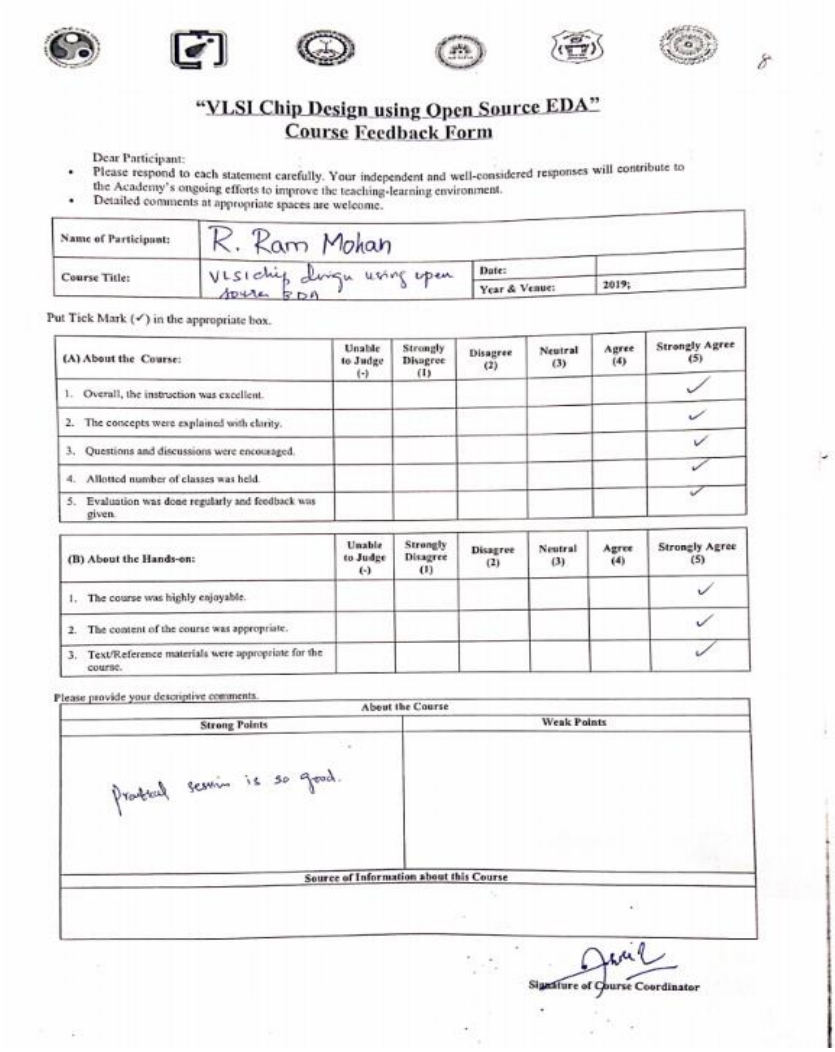
   Invited Talk 6 Dr. C. P. Ravikumar (Texas Instrument)

5. Venue of the Event: ECAD Lab, KKR and KSR Institute of Technology, Guntur, AP
6. Date & Time of the Event 08-07-2019 to 12-07-2019, 9 AM to 6 PM
7. No of Students participated: NIL

8. Year, Branch and Section of Students: NIL

9. No of Faculties participated:57

10. One Faculty Member Feed Back:



"VLSI Chip Design using Open Source EDA"
Course Feedback Form

Dear Participant:
- Please respond to each statement carefully. Your independent and well-considered responses will contribute to the Academy's ongoing efforts to improve the teaching-learning environment.
- Detailed comments at appropriate spaces are welcome.

Name of Participant:	R. Ram Mohan		
Course Title:	VLSI chip design using open source EDA	Date: Year & Venue:	2019;

Put Tick Mark (✓) in the appropriate box.

(A) About the Course:	Unable to Judge (-)	Strongly Disagree (1)	Disagree (2)	Neutral (3)	Agree (4)	Strongly Agree (5)
1. Overall, the instruction was excellent.						✓
2. The concepts were explained with clarity.						✓
3. Questions and discussions were encouraged.						✓
4. Allotted number of classes was held.						✓
5. Evaluation was done regularly and feedback was given.						✓

(B) About the Hands-on:	Unable to Judge (-)	Strongly Disagree (1)	Disagree (2)	Neutral (3)	Agree (4)	Strongly Agree (5)
1. The course was highly enjoyable.						✓
2. The content of the course was appropriate.						✓
3. Text/Reference materials were appropriate for the course.						✓

Please provide your descriptive comments.

About the Course	
Strong Points	Weak Points
Practical session is so good.	
Source of Information about this Course	

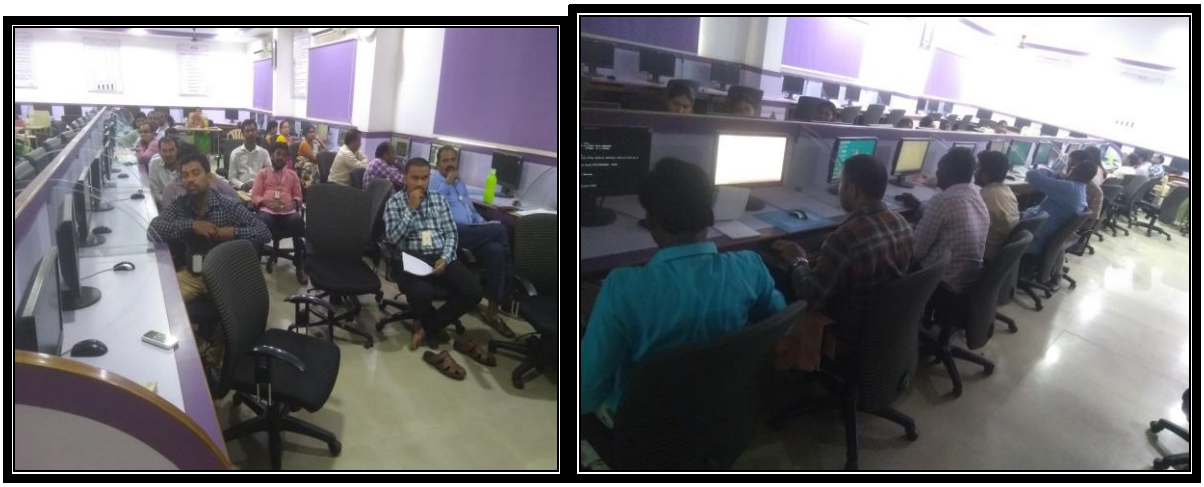
Signature of Course Coordinator

11. Promotion of the Event on the Social Media Website: (Link and Screenshot)

http://eict.iitg.ac.in/UpcomingSummerCourses19.html

2	**VLSI Chip Design Hands on using open source EDA** **08 - 12 July, 2019** NEW**Last Date of registration is 01/07/2019.** NEW**Last Date of registration is extended to 05/07/2019.** NEW**The Participation workshop will not be conducted tommorow.** NEW**Participants need to carry their laptops as it will be an interactive sessions.**	IIT Guwahati Dr. Gaurav Trivedi Email: trivedi@iitg.ac.in Mobile: 9435582802	**MNIT Jaipur** **Co-Principal Coordinator** Dr. C. Periasamy Email: cpsamy.ece@mnit.ac.in Mobile: 9549654235	**IIT Guwahati :** Dr. Gaurav Trivedi Email: trivedi@iitg.ac.in M: +91-9435582802 L:0361 2582536 **IIITDM Jabalpur :** Prof. P.N. Kondekar Email: pnkondekar@iiitdmj.ac.in Mobile: 9425805445 **MNIT Jaipur :** Dr. Chitrakant Sahu/Dr. Menka Yadav Email: chitrakant.ece@mnit.ac.in Mobile: 9549655371	Common Brochure Application Form(On-line) On-Spot registration is also available Schedule Coordinator Sensitization Workshop Participant Sensitization Workshop

12. Event Photographs from different angles covering all the students, Banner and speaker (Include 4 or 6 photographs in the Document and send those photos



13. 1- 2 minutes video of the event (Drive Link Only)

14. Benefit in terms of learning/Skill/Knowledge obtained *:

The following Modules are covered in the FDP Program

- SoC Design (RISC-V SoC, which implements RISC-V IMC ISA
- Pre-layout timing analysis (Lab - OpenSTA) and Floorplanning
- Placement, Clock tree synthesis, Routing and SI
- Post-layout STA
- ECO
- Important aspects, particular to Analog/Mixed signal IC design

15. Expenditure Amount (If any) : Rs 82,000/-Remarks:

16. Experiences and Output of the Session :

This course is designed to provide an exposure to the fundamentals of VLSI chip designing. Participants will learn Floor Planning, placement and global routing. Hands-on training and practice sessions will help participants gain confidence on Analog and Mixed Signal Circuits, their simulation and implementation including sessions on chip designing using EDA Tools. The course will be useful for faculty of engineering and sciences who are interested in the learning VLSI chip designing.