SYNCOM

ECE Dept. NEWS LETTER

VOICE OF ELECTRONIC AND COMMUNICATION ENGINEERING

November 2019 Vol.4 Issue 11

Editors:

Dr.Sk.Sadulla HOD-ECE
Mr.Maduguri Sudhir
Ms.Nuthalapati Soniya

Student Coordinators:

Mr.G.Saketh
Ms.V. Sri Hasitha
Mr.P.Komal VenkatSai
Ms.Ch.Naveena

VISION, MISSION &PEO'S

Vision

Developing highly Qualitative, Technically Competent and Socially Responsible Engineers.

Mission

To provide quality education in the domain of Electronics and Communication Engineering through

- Enriched curriculum for addressing the needs of Industry.
- Effective teaching learning processes through congenial environment.
- Gaining contemporary knowledge through research, development, curricular, co and extra-curricular.

ECE Program Educational Objectives

Graduates of Electronics & Communication EngineeringShall

PEO1: Develop a strong background in basic science and mathematics and ability to use these tools in their chosen fields of specialization.
PEO2: Have the ability to demonstrate technical competence in the fields of electronics and communication engineering and develop solutions to the problems.
PEO3: Attain professional competence through life-long learning such as advanced degrees, professional registration, and other professional activities.
PEO4: Function effectively in a multi-disciplinary environment and individually, within a global, societal, and environmental context.
PEO5: Take individual responsibility and to work as a part of a team towards the fulfillment of both individual and organizational goals.

The institute is a symbol of egalitarian outlook without discretions. KITS student activity council is organized exclusively by students with representatives from various disciplines stands for the advocacy of democracy and leadership opportunities provided by the institute.. **KITS imparts Outcome Based Education (OBE)** which gives equal opportunities to teaching and learning curricular, co-curricular and extra-curricular activities

WORK SHOP ON VLSI DESIGN

ECE Department conducted a three day workshop on **"VLSI DESIGN USING MENTOR GRAPHICS"** from 7th to 9th November 2019.

Mr. Nagendra Bandi Application Engineer Coreel Technologies was the resource person for this Seminar

The objective of the work shop on mentor graphics tool is to create awareness on new VLSI design technologies in semiconductor industry. For the semiconductor industry, each technology node presents new challenges in IC design and manufacture. Efficient heat removal from die in MCP/MCMs, stacked-die packages, 3D ICs, is critical and a limiting factor in the miniaturization of package geometries that support ever-more advanced mobile and Consumer Electronics applications. Thinner die result in greater on-die temperature variation, and in the case of multi-die products, greater die-die thermal interaction, such that IC design flows now need to be 'temperature aware'. LEDs present a unique challenge in terms of their thermal design and opto-thermal characterization. Hence for the all above design steps it is necessary to know about mentor graphics tool to design VLSI Circuits.

Hands-on labs:

- Setting ICstudio preferences
- Creating projects in ICstudio
- Project maintenance in ICstudio
- Schematic capture
- Setting up and running analog simulation
- Working with mixed-signal designs
- Simulating a mixed-signal design with ADMS
- Basic polygon editing skills
- Working with hierarchical layouts

- Automatically generating device layout and interconnection (SDL)
- Creating, sizing, and placing hierarchical blocks
- Finding layout design rule errors with Calibre DRC
- Verifying layout connectivity with Calibre LVS
- Extracting and simulating with parasitic data

Benefits to the Participants:

- Create and modify IC studio projects
- Create and edit hierarchical schematics
- Import HDL descriptions for design elements
- Set up and run analog simulations
- Create and simulate mixed-signal designs
- Create and edit hierarchical IC layouts
- Use Schematic-Driven Layout (SDL) tools to automatically construct layouts
- Add layout routing using interactive and automatic routing tools
- Plan top-level block size and placement using comprehensive floorplanning tools
- Verify layouts using Calibre DRC/LVS
- Extract parasitic data and use extracted parasitic data in simulations

All ECE Department Faculty members are attended the workshop by **Mr. Nagendra Bandi Application Engineer Coreel Technologies** on "**VLSI DESIGN USING MENTOR GRAPHICS**" on 7th to 9th November 2019, conducted by KKR & KSR Institute of Technology and Sciences in association with MHRD-IIC.

ONE DAY SEMINAR ON RECENT TRENDS IN RESEARCH & DEVELOPMENT

ECE Department conducted a seminar on **"Recent Trends in Research & Development"** On 15th November 2019. **Mr.A.Surendar R&D Head Synthesis hub, Coimbatore, Tamilnadu** was the resource person for this Seminar.

The main objective of this seminar is to help researchers to develop research skills and competencies, acquaint them with contemporary real life aspects of public administration, and improve the effectiveness of their independent research work, which is required for the successful preparation of the term paper and Master's thesis.

Seminar on Recent Trends in Research & Development objectives:

a) Professional orientation of researchers to help them choose the field and topic of their dissertation

b) Inculcating academic skills, including preparing and conducting research

c) Involving Researchers in project activities and R&D for government

d) Writing and publishing research papers and articles

e) Teaching researchers to gather, systematize, and process information and prepare analytic reports and documents

f) Acquainting researchers with the standard workflow in government bodies and public organizations

In addition, researchers combine their studies with research (particularly, with the Institute for Public Administration and Governance and Sales Management), conferences, seminars, research project competitions and work in research labs (such as the Centre for Studies of the Civil Society and Non-Profit Sector and the Laboratory for Interdisciplinary Research in the Non-Profit Sector). Apart from research seminars, researchers on the Programme participate in specific projects. They complete specific tasks set by the project owner, collect and assess data or provide expert analysis of a situation identified by the project owner. By attending this seminar participants got numerous benefits, including improving communication skills, gaining expert knowledge, networking with others and renewing motivation and confidence.

Oral Communication:

This seminar is so a comfortable, open environment for practicing professional communication techniques. This seminar helped participants to become a better listener, and to present arguments and ideas clearly and be open to others' points of view. Group discussions and activities also practiced, such as dealing with conflicting opinions among group members and working together to accomplish assignments or tasks.

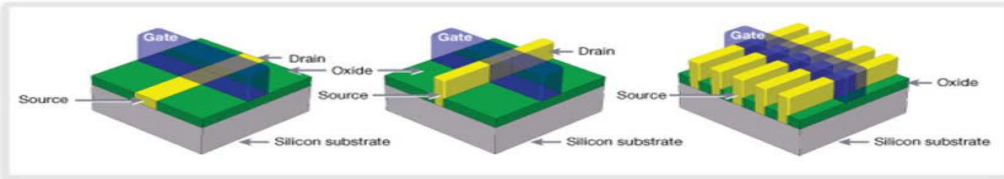
Expert Knowledge:

This seminar gave participants intensive exposure to a topic through presentations and discussions led by expert. This seminar is an ideal opportunity for people who want to study a topic in depth. By asking questions, taking detailed notes and being prepared for each events, participants left with a wide range of knowledge in a specific field.

Networking:

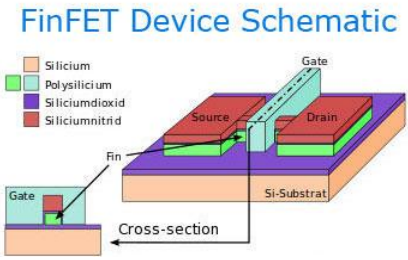
Along with having access to experts, this seminar also gives participants the opportunity to meet other people who share their interests. Seminar discussions offer chances to debate issues related to the field, share experiences and exchange perspectives. Learn Higher also states that meeting new people can offer encouragement, solutions to common problems and advice for how to handle challenges. These relationships can continue into professional connections even after the seminar is over.

All ECE Department Faculty members are attended the seminar by Mr. A.Surendar R&D Head in Synthesishub on “Resent trends in Research and Development” on 15th November 2019,



Faculty Article:

FinFET Transistor Technology



FinFET transistor technology is being used in many areas of IC technology where the 3D fins provide added density for same feature size.

FinFET technology has recently seen a major increase in adoption for use within integrated circuits. Compared to the more usual planar technology, FinFET transistor technology offers some significant advantages in IC design. The FinFET technology promises to provide the deliver superior levels of scalability needed to ensure that the current progress with increased levels of integration within integrated circuits can be maintained.

The FinFET offers many advantages in terms of IC processing that mean that it has been adopted as a major way forwards for incorporation within IC technology.

FinFET background

FinFET technology has been born as a result of the relentless increase in the levels of integration. The basic tenet of Moore's law has held true for many years from the earliest years of integrated circuit technology. Essentially it states that the number of transistors on a given area of silicon doubles every two years.

Some of the landmark chips of the relatively early integrated circuit era had a low transistor count even though they were advanced for the time. The 6800 microprocessor for example had just 5000 transistors. Todays have many orders of magnitude more.

To achieve the large increases in levels of integration, many parameters have changed. Fundamentally the feature sizes have reduced to enable more devices to be fabricated within a given area. However other figures such as power dissipation, and line voltage have reduced along with increased frequency performance.

There are limits to the scalability of the individual devices and as process technologies continued to shrink towards 20 nm, it became impossible to achieve the proper scaling of various device parameters. Those like the power supply voltage, which is the dominant factor in determining dynamic power were particularly affected. It was found that optimising for one variable such as performance resulted in unwanted compromises in other areas like power. It was therefore necessary to look at other more revolutionary options like a change in transistor structure from the traditional planar transistor.
One of the key issues is that as technologies use smaller feature sizes, the source and the drain of the MOS devices used encroach into the channel, making it easier for leakage current to flow between them and also making it very difficult to turn the transistor off completely.

FinFET basics:

FinFET technology takes its name from the fact that the FET structure used looks like a set of fins when viewed. In fact the FinFET gained its name from Profs. Chenming Hu, Tsu-Jae King-Liu and Jeffrey Bokor at the University of California, Berkeley who were the first to coin the term as a result of the shape of the structure.

FinFETs are 3d structures that rise above the substrate and resemble a fin. The 'fins' form the source and drain, effectively and in this way they enable more volume than a traditional planar transistor for the same area. The gate wraps around the fin, and this gives more control of the channel as there is sufficient length for the control. Also as the channel has been extended there is very little current to leak through the body when the device is in the 'off' state. This also allows the use of lower threshold voltages and it results in better performance and lower power dissipation.

The gate orientation is at right angles to the vertical fin. And to traverse from one side of the fin to the other it wraps over the fin, enabling it to interface with three side of the fin or channel.
This form of gate structure provides improved electrical control over the channel conduction and it helps reduce leakage current levels and overcomes some other short-channel effects..

The term FinFET is used somewhat generically. Sometimes it is used to describe any fin-based, multigate transistor architecture regardless of number of gates.

By/-T.Bhavani, Asst. prof.

Student Article:

The 6 Main Ways Technology Impacts Your Daily Life

We are living in an era of advanced technology, where every part of our daily lives is related to the science of craft in one way or another. There's no doubt that over the years technology has been responsible for creating amazingly useful resources which put all the information we need at our fingertips. The development of technology has led to so many mind-blowing discoveries, better facilities, and better luxuries, but at the same has dramatically changed our daily lives. Various highly-developed gadgets, connected to the Internet, have changed the way we communicate, use humor, study, work, shop, play, and behave.

1: Improved Communication

The continuous advances in technology have led to the appearance of numerous new methods of electronic communication, such as social networking websites, emails, voicemails, and video conferences. These advanced communication tech tools have helped us to eliminate time and distance as obstacles to effective communication. This is beneficial not only to our personal relationships, but also to education and business. Technology has improved cultural education by giving children the opportunity to communicate with other children from different countries and learn about different cultures.

2: Improved Home Entertainment

Not that long ago, our entertainment experiences used to live in the moment they happened, exist in our memories and find their way in old-fashioned photographs on wall. Today, that has all changed due to the rapid growth of the Internet, mobile connectivity, and social networks.

One of the biggest changes, for example, was the switch from videotapes to CDs/DVDs. This enabled manufacturers to put more data onto the medium. This meant that there were no risks of the tape coming out of the player and getting damaged that easily, and due to the small size of the DVDs, it also meant that a lot more could be stored in the same amount of space.

3: Improved Housing and Lifestyle

Housing and lifestyle have also been impacted by the modern technology. The majority of the items that you have in your home today are automated, which makes your life much easier, organized and safer. Thanks in particular to the advanced technological solutions such automated door locks, security cameras and lighting control, our homes are now more secure than ever. Also, thanks to the Internet, we have an easy access to all sorts of information, news, and you're able to shop online any time of the day or night from the comfort of your own home.

4: Changed Health Industry

There's no doubt that technology is the driving force behind the huge improvements in healthcare. The majority of the hospitals today have implemented modern technology in hospitals and surgical rooms, which has significantly reduced the mistakes made by doctors. The increased accessibility of treatment is also one of the most amazing ways that technology has changed health care. Besides the technological advancements in hospitals, there are also many health phone and desktop apps that allow you to easily monitor your weight, heart rate, and other health properties at any time of the day. Needless to say, the Internet is our main source of medical information.

5: Convenience in Education

Technology has impacted every aspect of our lives today, and education is no exception. Technology has changed education in so many ways. First, technology has expanded the access to education and there are huge amounts of information (books, images, videos, audio) that are available through the Internet and that will enable you to empower yourself with knowledge. In addition, online courses are on the rise and most of them are free.

6: Convenience of Traveling

Modern transportation technology has made it easier for individuals to travel long distances. Since transport is an important part of our lives, technology has been regularly working on making it more efficient and quicker. The first steamship was built in the 1770s, the first steam-powered train was built in 1798, and the modern car was created in 1886, while the first powered, controlled flight is believed to have taken place in 1903.

By/-Ms.Ch.Naveena (II ECE)

We are proudly announcing that 3 of our students got placed in ZenQ.

Your ability has taken you to the new height of success, this great job is all because of your dedication and hard work and yes confidence too, many congrats to you, stay blessed!

You may have been lucky to get your new job, but We think that your company is much luckier to get you as a new employee. Good luck.

Ms.DUMPALA LAKSHMI PRASANNA (16JR1A0414) got placed in ZenQ placement Drive.

Wishing you good luck with your new job. May this new job takes you to the way of success in the journey of success!

Ms. VIPPARLA VENKATA SAI VASANTHA (16JR1A04D9) got placed in ZenQ placement Drive.

We are so happy for you my friend. It's our complete faith on you that you have the power to achieve a bright future in your career.

Ms. GANAPAM SUSHMA (16JR1A0418) got placed in ZenQ placement Drive.

Sending you a ton of best wishes on a great achievement of yours. May you do awesome and be succeeding to complete the target in your new job.

FACULTY ACHIEVEMENTS

Dr.Sk.Sadulla attended for a three day workshop on **"VLSI DESIGN USING MENTOR GRAPHICS"** from 7th to 9th November 2019.With his interest he attended for a seminar **"Recent Trends in Research & Development"** On 15th November 2019.

Prof. K. Madhu Sudhana Rao attended for a three day workshop on **"VLSI DESIGN USING MENTOR GRAPHICS"** from 7th to 9th November 2019.With his interest he attended for a seminar **"Recent Trends in Research & Development"** On 15th November 2019.

Prof. V. Murali Krishna attended for a three day workshop on **"VLSI DESIGN USING MENTOR GRAPHICS"** from 7th to 9th November 2019.With his interest he attended for a seminar **"Recent Trends in Research & Development"** On 15th November 2019.

Dr.M.Vasim Babu attended for a three day workshop on **"VLSI DESIGN USING MENTOR GRAPHICS"** from 7th to 9th November 2019.With his interest he organized a seminar **"Recent Trends in Research & Development"** On 15th November 2019.

Dr. Sk. Khmuruddeen attended for a three day workshop on **"VLSI DESIGN USING MENTOR GRAPHICS"** from 7th to 9th November 2019.With his interest he attended for a seminar **"Recent Trends in Research & Development"** On 15th November 2019.

Dr.M.Rambabu Naik attended for a three day workshop on **"VLSI DESIGN USING MENTOR GRAPHICS"** from 7th to 9th November 2019.With his interest he attended for a seminar **"Recent Trends in Research & Development"** On 15th November 2019.

Mr. M.Nagaraju ,Asst. Prof attended for a three day workshop on **"VLSI DESIGN USING MENTOR GRAPHICS"** from 7th to 9th November 2019.With his interest he attended for a seminar **"Recent Trends in Research & Development"** On 15th November 2019.

Mr. G.Malyadri ,Asst. Prof attended for a three day workshop on **"VLSI DESIGN USING MENTOR GRAPHICS"** from 7th to 9th November 2019.With his interest he attended for a seminar **"Recent Trends in Research & Development"** On 15th November 2019.

Mrs. T.Bhavani, Asst. Prof attended for a three day workshop on **"VLSI DESIGN USING MENTOR GRAPHICS"** from 7th to 9th November 2019.With her interest she attended for a seminar **"Recent Trends in Research & Development"** On 15th November 2019.

- Presented a paper on **"Investigation on EBG structured CPW fed CM antenna for WiMAX, WLAN Applications**" in International Conference on Vision towards Emerging Trends in Communication and Networking, ViTECoN 2019.
- Attended for a Two Week FDP from 4th to 15th November 2019 on **"Mixed Signal Design"** conducted by VVIT Guntur.

Mr. E.Venkata Narayana attended for a three day workshop on **"VLSI DESIGN USING MENTOR GRAPHICS"** from 7th to 9th November 2019.With his interest he attended for a seminar **"Recent Trends in Research & Development"** On 15th November 2019.

Mr. Maduguri Sudhir ,Asst. Prof attended for a three day workshop on **"VLSI DESIGN USING MENTOR GRAPHICS"** from 7th to 9th November 2019.With his interest he attended for a seminar **"Recent Trends in Research & Development"** On 15th November 2019.

Mr. T.Venkat Rao ,Asst. Prof attended for a three day workshop on **"VLSI DESIGN USING MENTOR GRAPHICS"** from 7th to 9th November 2019.With his interest he organized a seminar **"Recent Trends in Research & Development"** On 15th November 2019.

Mr.K. Mallikarjuna Rao,Asst. Prof attended for a three day workshop on **"VLSI DESIGN USING MENTOR GRAPHICS"** from 7th to 9th November 2019.With his interest he attended for a seminar **"Recent Trends in Research & Development"** On 15th November 2019.

Mr. B.Venu ,Asst. Prof attended for a three day workshop on **"VLSI DESIGN USING MENTOR GRAPHICS"** from 7th to 9th November 2019.With his interest he attended for a seminar **"Recent Trends in Research & Development"** On 15th November 2019.

Mrs. P.Sarala ,Asst. Prof attended for a three day workshop on **"VLSI DESIGN USING MENTOR GRAPHICS"** from 7th to 9th November 2019.With her interest she attended for a seminar **"Recent Trends in Research & Development"** On 15th November 2019.

➢Published a paper on **"Beamforming with Precoders Based Millimeter Wave Communication System**" in International Journal of Innovative Technology and Exploring Engineering(IJITEE), November 2019.

Mr. K.Murali Krishna ,Asst. Prof attended for a three day workshop on **"VLSI DESIGN USING MENTOR GRAPHICS"** from 7th to 9th November 2019.With his interest he attended for a seminar **"Recent Trends in Research & Development"** On 15th November 2019.

Ms. N.Soniya ,Asst. Prof attended for a three day workshop on **"VLSI DESIGN USING MENTOR GRAPHICS"** from 7th to 9th November 2019.With her interest she attended for a seminar **"Recent Trends in Research & Development"** On 15th November 2019.

Mr. M.Venu ,Asst. Prof attended for a three day workshop on **"VLSI DESIGN USING MENTOR GRAPHICS"** from 7th to 9th November 2019.With his interest he attended for a seminar **"Recent Trends in Research & Development"** On 15th November 2019.

Mr. P.Ashok Babu ,Asst. Prof attended for a three day workshop on **"VLSI DESIGN USING MENTOR GRAPHICS"** from 7th to 9th November 2019.With his interest he attended for a seminar **"Recent Trends in Research & Development"** On 15th November 2019.

Mr. M.Madhusudhan Reddy ,Asst. Prof organized a three day workshop on **"VLSI DESIGN USING MENTOR GRAPHICS"** from 7th to 9th November 2019.With his interest he attended for a seminar **"Recent Trends in Research & Development"** On 15th November 2019.

Mrs. K.Sowjanya ,Asst. Prof attended for a three day workshop on **"VLSI DESIGN USING MENTOR GRAPHICS"** from 7th to 9th November 2019.With her interest she attended for a seminar **"Recent Trends in Research & Development"** On 15th November 2019.

Mr. R.Rammohan ,Asst. Prof attended for a three day workshop on **"VLSI DESIGN USING MENTOR GRAPHICS"** from 7th to 9th November 2019.With his interest he attended for a seminar **"Recent Trends in Research & Development"** On 15th November 2019.

Mr. B.Brahmaiah ,Asst. Prof attended for a three day workshop on **"VLSI DESIGN USING MENTOR GRAPHICS"** from 7th to 9th November 2019.With his interest he attended for a seminar **"Recent Trends in Research & Development"** On 15th November 2019.

Mr. G.Yaswanth ,Asst. Prof attended for a three day workshop on **"VLSI DESIGN USING MENTOR GRAPHICS"** from 7th to 9th November 2019.With his interest he attended for a seminar **"Recent Trends in Research & Development"** On 15th November 2019.

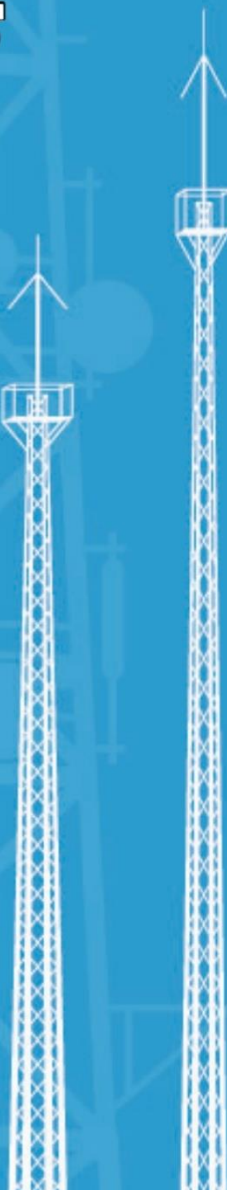
Mr. S.Sudharshan Reddy ,Asst. Prof attended for a three day workshop on **"VLSI DESIGN USING MENTOR GRAPHICS"** from 7th to 9th November 2019.With his interest he attended for a seminar **"Recent Trends in Research & Development"** On 15th November 2019.

Ms. P.Jwalitha, Asst. Prof attended for a three day workshop on **"VLSI DESIGN USING MENTOR GRAPHICS"** from 7th to 9th November 2019.With her interest she attended for a seminar **"Recent Trends in Research & Development"** On 15th November 2019.

Ms. K.Leela Rani ,Asst. Prof attended for a three day workshop on **"VLSI DESIGN USING MENTOR GRAPHICS"** from 7th to 9th November 2019.With her interest she attended for a seminar **"Recent Trends in Research & Development"** On 15th November 2019.

THE ART OF COMMUNICATION IS THE LANGUAGE OF LEADERSHIP....

- James Humes



KITS KKR & KSR INSTITUTE OF TECHNOLOGY & SCIENCES

Department of Electronics and Communication Engineering