Code No: R1621042 **R16** SET - 1

II B. Tech I Semester Regular/Supplementary Examinations, October/November - 2019
SWITCHING THEORY AND LOGIC DESIGN
(Com to ECE, EIE and ECC)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1.	a)	What do you mean by Weighted code? Give examples.	(3M)
	b)	Define the Boolean function.	(2M)
	c)	List the applications of Multiplexers	(3M)
	d)	What are the merits of PAL.?	(2M)
	e)	What are the differences between synchronous and asynchronous sequential circuits	(2M)
	f)	Write the procedure for state diagram reduction?	(2M)

PART -B

2.	a)	Convert the following numbers into decimal numbers i) 1011011101101110_2 ii) $A0CB.EE_{16}$	(7M)
	b)	Perform the subtraction (-6) - (-13) using signed 2's complement representation.	(7M)
3.	a)	For the given Boolean function F=x y' z + x' y' z +w' x y + w x' y + w x y i. Simplify the function to minimal literals using Boolean algebra. ii. Construct the logic diagram using only NOR gates	(7M)
	b)	Reduce the expression using K-map $\sum m(0,1,4,5,7,9,11,15)+d(10,14)$.	(7M)
4.	a)	Design a circuit to convert Excess-3 code to BCD code using discrete Logic gates.	(7M)
	b)	Realize the Boolean function F= $\Sigma(1,2,5,7)$ using (i) 8x1 multiplexer (ii) 4x1 multiplexer	(7M)
5.	a)	Specify the size of a ROM (number of words and numbers bits per word) that will accommodate the truth table of a BCD to seven segment decoder with an enable input and draw the logic diagram.	(7M)
	b)	Design a BCD to Excess-3 code converter and implement using suitable PLA.	(7M)
6.	a)	What do you mean by triggering? Explain the various triggering modes with examples.	(7M)
	b)	Design Mod-10 Counter using T Flip-Flops.	(7M)
7.	a)	Draw the logic diagram of Meelay and Moore models and also explain their operation with examples	(7M)
	b)	Explain the minimization procedure for determining the set of equivalent state of a specified machine M.	(7M)
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PART –A

1. a) Define 2421 code. (2M)
   b) State De-morgan theorems (3M)
   c) What is encoder? Give examples. (2M)
   d) Give the comparison between PLA and PAL. (2M)
   e) What are the differences between Latches and Flip Flops (2M)
   f) What are the limitations of FSM? (3M)

PART -B

2. a) Explain different methods used to represent negative numbers in binary system. (7M)
   b) Write the following binary numbers in signed 1's complement form and signed 2's complement form using 16 bit registers. (7M)
   (i) +1001010 (ii) -11110000 (iii) -11001100.1 (iv) +100000011.111

3. a) Obtain the complement of the following Boolean expressions. (4M)
   (i) AB+A(B+C)+B'(B+D) (ii) A+B+A'B'C
   b) Simplify the function $F(w, x, y, z) = \Sigma(1,3,7,11,15)$, which has the don't care conditions $d(w, x, y, z) = \Sigma(0,2,5)$ using Karnaugh map (10M)

4. a) Explain the priority encoder with a neat logic diagram. (7M)
   b) Explain the operation of a look ahead adder circuit with neat diagram (7M)

5. a) Tabulate the PLA programming table for the four Boolean functions listed below (7M)
   $A(x,y,z) = \Sigma (1, 2, 4, 6)$ $B(x,y,z) = \Sigma (0, 1, 6, 7)$
   $C(x,y,z) = \Sigma (2,6)$ $D(x,y,z) = \Sigma (1, 2, 3, 5, 7)$
   b) Design a BCD to seven segment decoder using PROM (7M)

6. a) Draw the logic diagram of a JK flip flop and using excitation table. explain its operation. (7M)
   b) Draw the circuit diagram of Johnson counter using D-flip-flops and explain its operation with the help of bit pattern. (7M)
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7. a) Discuss Mealay Machine models of sequential circuits. (4M)

   b) Convert the following Mealay machine into a corresponding Moore machine. (10M)

Present State	Input , X=0 Next state, output	Input , X=1 Next state, output
A	B, 0	E, 0
B	E, 0	D, 0
C	D, 1	A, 0
D	C,1	E, 0

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PART –A

1.	a)	Concert $(0.513)_{10}$ to octal	(3M)
	b)	Obtain the dual of A'B+A'BC'+A'BCD+A'BC'D'E	(2M)
	c)	What is binary subtractor?	(2M)
	d)	Give the basic structure of PLA.	(3M)
	e)	What is Race around condition?	(2M)
	f)	What is a state diagram?	(2M)

PART -B

2.	a)	Represent $(199)_{10}$ in the following code: (i) Binary (ii) BCD (iii) 2421 (iv) 84-2-1.	(8M)
	b)	Convert the following. i. $AB_{16} = (\ )_{10}$ ii. $1234_8 = (\ )_{10}$ iii. $10110011_2 = (\ )_{10}$	(6M)
3.	a)	Simplify the following Boolean function to a minimum number of literals. F (A, B, C)= $\sum(1,4,5,6,7)$.	(4M)
	b)	For the given function F(A, B, C, D, E) =Σ(0,1, 2, 3, 4, 5, 9, 10, 16, 17, 18, 19, 20, 22, 25, 26)+ Σd (7, 11, 12, 13, 15, 23, 27, 28, 29, 30). Obtain minimal SOP expression using K-Map.	(10M)
4.	a)	Explain how a decoder can be converted into a de-multiplexer with relevant block diagrams and truth tables.	(7M)
	b)	Realize a 3 to 8 decoder using 2 to 4 decoder and other required gates.	(7M)
5.	a)	Implement the following Boolean functions using a PAL that has four sections with three product terms each. F1 (A, B, C, D) = ∑ (2, 12, 13) and F2 (A, B, C, D) = ∑ (7, 8, 9, 10, 11, 12, 13, 14, 15)	(10M)
	b)	Compare PROM, PLA and PAL.	(4M)
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6. a) Using the method of flip flop conversion carry out the conversion from JK flip flop to D flip flop. (7M)
   b) Design a decade counter using RS flip flops. (7M)

7. a) Distinguish between Meelay & Moore machines (4M)
   b) Design a Moore type sequence detector to detect a serial input sequence of 101. (10M)

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PART –A

1.	a)	Concert $(0.513)_{10}$ to hexadecimal	(3M)
	b)	Obtain the Complement of ABEF+ABE'F'+A'B'EF	(2M)
	c)	What are the applications of full adders?	(2M)
	d)	Describe a programming table with respect to PLDS.	(3M)
	e)	What is toggle condition in a flip flop?	(2M)
	f)	What is the significance of reduction of state tables.	(2M)

PART -B

2.	a)	Implement the function F(A,B,C,D) = ∑m(0,2,3,4,6,7,9,10,12,15) with the following four level forms. i) NAND-AND ii) NOR-OR iii) OR –AND.	(6M)
	b)	Given the 8-bit data word 10111001, generate the 12-bit composite word for the Hamming code that corrects and detects signals error.	(8M)
3.	a)	Simplify the following Boolean function using K –Map method in POS form. F=Π(2,3,4,6,9,11,12,13).	(7M)
	b)	Simplify the following Boolean function using Tabulation method. Y(A,B,C,D) = Σ(1,3,5,8,9,11,15)	(7M)
4.	a)	Design a 4 bit carry look ahead adder circuit.	(7M)
	b)	Implement 64 × 1 multiplexer with four 16 × 1 and one 4 ×1 multiplexer (use only block diagram).	(7M)
5.	a)	Given a 32 x 8 Rom chip with an enable input, show the external connection necessary to construct a 128 x 8 Rom with four chips and a decoder.	(10M)
	b)	Explain the merits & demerits of PROM	(4M)
6.	a)	Draw the logic diagram of RS flip flop and explain its operation.	(7M)
	b)	Design a 4 bit ring counter using D flip-flops and explain its operation with the help of bit pattern.	(7M)
7.	a)	Explain the following related to sequential circuits with suitable examples. a)State diagram b)State assignment	(8M)
	b)	Discuss Moore Machine models of sequential circuits.	(6M)
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