JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY: KAKINADA

KAKINADA – 533 003, Andhra Pradesh, India

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

II Year - I Semester		L	T	P	C
		0	0	3	1.5
	SWITCHING THEORY and LOGIC DESIGN LAB				

List of Experiments: (Minimum of Twelve Experiments has to be performed)

1. Verification of truth tables of Logicgates
   Two input (i) OR (ii) AND (iii) NOR (iv) NAND (v) Exclusive OR (vi) Exclusive NOR
2. Design a simple combinational circuit with four variables and obtain minimal SOP expression and verify the truth table using Digital TrainerKit
3. Verification of functional table of 3 to 8 line Decoder /De-multiplexer
4. 4 variable logic function verification using 8 to 1multiplexer.
5. Design full adder circuit and verify its functionaltable.
6. Verification of functional tablesof
   (i) J K Edge triggered Flip –Flop
   (ii) J K Master Slave Flip – Flop
   (iii)D Flip -Flop
7. Design a four bit ring counter using D Flip – Flops / JK Flip Flop and verifyoutput
8. Design a four bit Johnson's counter using D Flip-Flops / JK Flip Flops and verifyoutput
9. Verify the operation of 4-bit Universal Shift Register for different Modes ofoperation.
10. Draw the circuit diagram of MOD-8 ripple counter and construct a circuit using T-Flip-Flops and Test it with a low frequency clock and Sketch the outputwaveforms.
11. Design MOD – 8 synchronous counter using T Flip-Flop and verify the result and Sketch the outputwaveforms.
12. (a) Draw the circuit diagram of a single bit comparator and test theoutput
    (b) Construct 7 Segment Display Circuit Using Decoder and 7 Segment LED and testit.

ADD on Experiments:
1. Design BCD Adder Circuit and Test the Same using RelevantIC
2. Design Excess-3 to 9-Complement convertor using only four Full Adders and test the Circuit.
3. Design an Experimental model to demonstrate the operation of74154 De-Multiplexer using LEDs foroutputs.