Code No: R1632043 **R16** SET - 1

III B. Tech II Semester Regular Examinations, April/May - 2019

VLSI DESIGN

(**Common to** Electronics and Communication Engineering, Electronics and Instrumentation Engineering, Electronics and Computer Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1.	a)	Write down the equations for I_{ds} of an n-channel enhancement MOSFET operating in Non-saturated region and saturated region.	[2M]
	b)	Define stick diagram and layout diagram.	[2M]
	c)	Explain about the constraints in choice of layers.	[2M]
	d)	Mention the common techniques involved in ad-hoc testing.	[3M]
	e)	What information from the targeted FPGA device is required in RTL synthesis?	[3M]
	f)	Explain about clock skew.	[2M]

PART -B

2.	a)	Explain the nMOS enhancement mode fabrication process for different conditions of V_{ds}.	[7M]
	b)	Derive an expression for transconductance of an n-channel enhancement MOSFET operating in active region.	[7M]
3.	a)	Draw a stick diagram and layout for two input CMOS NAND gate indicating all the regions and layers.	[7M]
	b)	Explain 2 µm Double Metal, Double Poly CMOS / BiCMOS Rules.	[7M]
4.	a)	Explain the issues involved in driving large capacitor loads in VLSI circuit regions.	[7M]
	b)	Calculate the gate capacitance value of 5 mm technology minimum size transistor with gate to channel value is 4×10^{-4} pF/mm^2.	[7M]
5.	a)	Explain about the following types of faults with suitable example: (i) stuck at faults (ii) Bridge faults (iii) temporary faults	[7M]
	b)	Explain the different categories of DFT techniques.	[7M]
6.	a)	Write down the step by step approach for FPGA design process on XILINX environment?	[7M]
	b)	Draw and explain the basic architecture of FPGA.	[7M]
7.	a)	Explain about deep submicron processes with suitable schematic diagrams.	[7M]
	b)	Explain about the scaling limitation for low voltage, low power design. Give the effect of scaling on various MOSFET parameters with necessary equations.	[7M]

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Code No: R1632043 **R16** SET - 2

III B. Tech II Semester Regular Examinations, April/May - 2019

VLSI DESIGN

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Time: 3 hours Max. Marks: 70

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2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1.	a)	Explain the terms SSI, LSI, and VLSI with the number of transistors per chip and applications.	[2M]
	b)	Draw the stick diagram for CMOS Inverter.	[2M]
	c)	What is sheet resistance? Derive the Expression for R_S?	[2M]
	d)	What are the approaches in design for testability?	[3M]
	e)	Explain synthesis process.	[3M]
	f)	What are the different types of power consumption?	[2M]

PART -B

2.	a)	Explain in detail the p-well process for CMOS fabrication indicating the masks used.	[7M]
	b)	Compare the relative merits of three different forms of pull-up for an inverter circuit. What is the best choice for realization in nMOS and CMOS technology?	[7M]
3.	a)	What are the λ-based design rules? Give them for each layer.	[7M]
	b)	Draw a stick diagram for CMOS logic $Y= (A+B+C)'$.	[7M]
4.	a)	What is inverter delay? How delay is calculated for multiple stages? Explain.	[7M]
	b)	Two nMOS inverters are cascaded to drive a capacitive load $C_L=16C_g$. Calculate pair delay V_{in} to V_{out} in terms of τ.	[7M]
5.	a)	What are the different faults found in combinational circuits? How can they be categorized?	[7M]
	b)	Briefly discuss about Built-In-Self Test technique with a suitable diagram.	[7M]
6.	a)	Give the steps in FPGA design flow with flow diagram and briefly discuss about each step.	[7M]
	b)	Explain about the principle and operation of FPGAs. What are its applications?	[7M]
7.	a)	Discuss about the various problems associated with low voltage VLSI circuit design.	[7M]
	b)	Explain about estimation and optimization of switching activity.	[7M]

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Code No: R1632043 **R16** SET - 3

III B. Tech II Semester Regular Examinations, April/May - 2019

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Time: 3 hours Max. Marks: 70

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2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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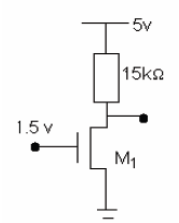
PART –A

1.	a)	Define Moore's law.	[2M]
	b)	Draw a symbolic layout of a two–input NAND gate.	[3M]
	c)	Give the scaling factor for Maximum operating frequency (f_0) in terms of different scaling models.	[2M]
	d)	What is meant by observability?	[3M]
	e)	What are FPGAs?	[2M]
	f)	What is switching activity?	[2M]

PART -B

2.	a)	Compare BiCMOS technology with other Technologies.	[7M]
	b)	Calculate I_D and V_{DS} if k_n = 100 μA/v^2, V_{tn} = 0.6V and W/L =3 for transistor M_1, in the circuit shown below:	[7M]



3.	a)	Explain with suitable examples how to design the layout of a Gate to maximize performance and minimize area.	[7M]
	b)	Design a stick diagram for nMOS logic Y= $(A+B+C)'$.	[7M]
4.	a)	How does depletion regions around source and drain are affected due to scaling down of device dimensions? Explain.	[7M]
	b)	Derive the expression for propagation delay in the case of cascaded pass transistors.	[7M]
5.	a)	Define the terms 'failure' and 'fault'. Discuss the different fault models.	[7M]
	b)	Briefly discuss about On-Chip clock generation and distribution.	[7M]
6.	a)	Explain the following terms: (i) LUT (ii) CLB (iii) IOB (iv) Switch matrix	[8M]
	b)	List out the various FPGA families. Explain how they are different from each other?	[6M]
7.	a)	Explain about the design limitations imposed on low power, low voltage circuits pertaining to the scaling and inter connect wires.	[7M]
	b)	Briefly discuss about the different techniques for reduction of switching capacitance.	[7M]

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Code No: R1632043 **R16** SET - 4

III B. Tech II Semester Regular Examinations, April/May - 2019

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Time: 3 hours Max. Marks: 70

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2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1.	a)	Discuss the microelectronics evolution.	[3M]
	b)	What is Vias? How to construct it in layout?	[2M]
	c)	What is the need of scaling in MOS circuits?	[2M]
	d)	Explain how function of system can be tested.	[2M]
	e)	List out the commercially available FPGAs.	[3M]
	f)	What is the need of interconnect?	[2M]

PART -B

2.	a)	What are the additional two layers in BiCMOS technology compared to others? With neat sketches explain BiCMOS fabrication process.	[7M]
	b)	Show that the switching speed of an enhancement MOSFET varies inversely as the square of the channel length.	[7M]
3.	a)	Give the design rules for the following cases with neat sketches: (i) Polysilicon – polysilicon (ii) n-type diffusion – n-type diffusion (iii) n-type diffusion – p-type diffusion (iv) metal 1 – metal 2.	[8M]
	b)	Design a stick diagram for two input pMOS NAND and NOR gates.	[6M]
4.		Describe the following briefly (i) Cascaded inverters as drivers (ii) Super buffers (iii) BiCMOS drivers	[14M]
5.	a)	Explain the terms controllability, observability and fault coverage.	[7M]
	b)	With suitable diagrams, explain the Scan based test techniques.	[7M]
6.	a)	List out the different configuration modes in FPGA. Briefly discuss about it.	[7M]
	b)	How the pass transistors are used to connect wire segments for the purpose of FPGA programming? Explain.	[7M]
7.	a)	What is the different technical parameter issues connected with VLSI low power and low voltage design? Explain.	[7M]
	b)	With schematic diagrams explain about deep submicron processes.	[7M]

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