

## **KKR&KSR Institute of Technology and Sciences Vinjanampadu, Guntur, Andhra Pradesh-522017**

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Accredited with "A" Grade by NAAC & NBA Accreditation Status for 4 UG (CSE, ECE, EEE, ME) Programs

### **MHRD- IIC Report Format**

#### **NAME OF THE EVENT:**

#### **A THREE DAY WORK SHOP ON VLSI DESIGN USING MENTOR GRAPHICS**

##### 1. Objective of the Event:

The objective of the work shop on mentor graphics tool is to create awareness on new VLSI design technologies in semiconductor industry. For the semiconductor industry, each technology node presents new challenges in IC design and manufacture. Efficient heat removal from die in MCP/MCMs, stacked-die packages, 3D ICs, is critical and a limiting factor in the miniaturization of package geometries that support ever-more advanced mobile and Consumer Electronics applications. Thinner die result in greater on-die temperature variation, and in the case of multi-die products, greater die-die thermal interaction, such that IC design flows now need to be 'temperature aware'. LEDs present a unique challenge in terms of their thermal design and opto-thermal characterization. Hence for the all above design steps it is necessary to know about mentor graphics tool to design VLSI Circuits.

##### 2. About the Program/Event:

This Program will provide all the knowledge needed to apply the power of IC studio, Mentor's integrated IC design environment, to most challenging VLSI designs. As participants progress through the course they will acquire the skills needed to manage their IC design project, capture and simulate their design, create the layout for their chip, use advanced interactive and automatic routing and floor planning tools, perform DRC and LVS verification, and use extracted parasitic data in post-layout simulation. The program addresses both analog and mixed-signal designs and provides everything in this comprehensive IC design environment.

#### **Hands-on labs**

- Setting ICstudio preferences
- Creating projects in ICstudio
- Project maintenance in ICstudio
- Schematic capture
- Setting up and running analog simulation

- Working with mixed-signal designs
  - Simulating a mixed-signal design with ADMS
  - Basic polygon editing skills
  - Working with hierarchical layouts
  - Automatically generating device layout and interconnection (SDL)
  - Creating, sizing, and placing hierarchical blocks
  - Finding layout design rule errors with Calibre DRC
  - Verifying layout connectivity with Calibre LVS
  - Extracting and simulating with parasitic data
3. Details of External Participants (If any): Nil
  4. Details of Resource Person :  
**Nagendra Bandi**  
**Application Engineer**  
**Email: [nagendra.b@coreel.com](mailto:nagendra.b@coreel.com)**  
**Mob: +91-9000234865**  
**Coreel Technologies – New Delhi**
  5. Venue of the Event: **ECAD LAB, KITS**
  6. Date & Time of the Event: **7<sup>th</sup> to 9<sup>th</sup> November 2019.**
  7. No of Students participated: **NIL**
  8. Department of Participants: **ECE**
  9. No of Faculties participated: **38**
  10. One Participant Feed Back:

I am K.Mallikarjuna Rao, working as an assistant professor in ECE department in KKR &KSR Institute of Technology and Sciences. I have attended the 3days Workshop on “**VLSI DESIGN USING MENTOR GRAPHICS**” First of all I want to thank my college management who provided such facility for all of us to learn and experience these workshops. In this regard my sincere thanks to AICTE-MHRD-IIC, who have been conducting such type of events for the faculty and student nourishment. We attended the workshop on on 7th to 9<sup>th</sup> November 2019. I learn the following kwy concepts from the workshop conducted on Mentor graphics.

**Key topics**

- ICstudio core concepts
- Project management with ICstudio

- Design Arcgitect-IC schematic capture environment
- Creating and editing schematics
- Setting up and running analog simulation
- Schematic capture - advanced topics
- Mixed-signal simulation
- IC Station overview
- IC Station polygon editing
- IC Station hierarchical editing
- Schematic-Driven Layout (SDL) in IC Station
- Interactive layout routing with IRoute
- Automatic routing with ARoute
- Floorplanning with ICassemble
- Layout verification with Calibre DRC/LVS
- Parasitic extraction with Calibre xRC

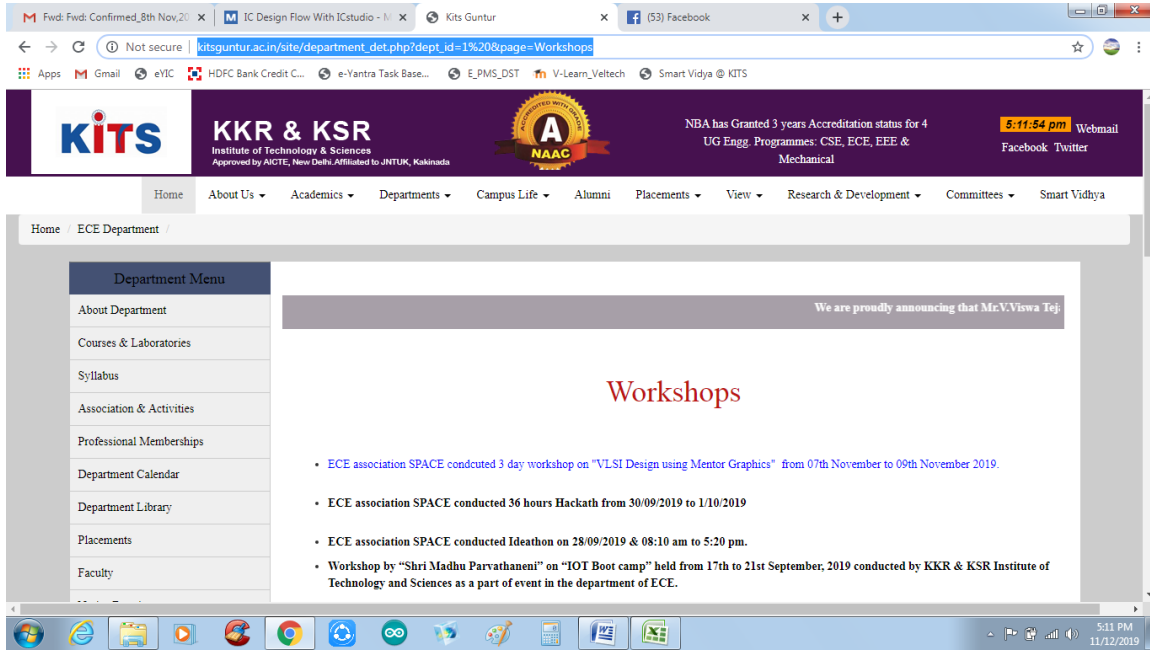
## 11. Promotion of the Event on the Social Media Website: (Link and Screenshot):

<https://www.facebook.com/photo.php?fbid=152908286107152&set=pcb.152908379440476&type=3&theater>



12. Promotion of the Event on the University/college Website :( Link and Screenshot)

[http://kitsguntur.ac.in/site/department\\_det.php?dept\\_id=1%20&page=Workshops](http://kitsguntur.ac.in/site/department_det.php?dept_id=1%20&page=Workshops)



13. Event Photographs from different angles covering all the students, Banner and speaker (Include 4 or 6 photographs in the Document and send those photos





14. 1- 2 minutes video of the event (Drive Link Only):

[https://drive.google.com/file/d/0B\\_xJgK3E0v2Y3Y1bXg1c3IRT2IVZHIGOU9ieWNGeDR4dWI0/view](https://drive.google.com/file/d/0B_xJgK3E0v2Y3Y1bXg1c3IRT2IVZHIGOU9ieWNGeDR4dWI0/view)

15. Benefit in terms of learning/Skill/Knowledge obtained \*: (Not Less than 1000 words)

**Benefits to the Participants**

- Create and modify IC studio projects
- Create and edit hierarchical schematics
- Import HDL descriptions for design elements
- Set up and run analog simulations
- Create and simulate mixed-signal designs
- Create and edit hierarchical IC layouts
- Use Schematic-Driven Layout (SDL) tools to automatically construct layouts
- Add layout routing using interactive and automatic routing tools
- Plan top-level block size and placement using comprehensive floorplanning tools
- Verify layouts using Calibre DRC/LVS
- Extract parasitic data and use extracted parasitic data in simulations

16. Expenditure Amount ( If any): **RS.25,000**

17. Remarks: The workshop is organized smoothly with practical orientation.

18. Experiences and Output of the Session

All ECE Department Faculty members are attended the workshop by **Mr. Nagendra Bandi Application Engineer Coreel Technologies** on “**VLSI DESIGN USING MENTOR GRAPHICS**” on 7<sup>th</sup> to 9<sup>th</sup> November 2019, conducted by KKR & KSR Institute of Technology and Sciences in association with MHRD-IIC.

**Outcomes of the Session**

**Mr. Nagendra Bandi Application Engineer Coreel Technologies** as a resource person a work shop on “Applications of LABVIEW in Engineering ” is organized. The session is Very



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useful and informative. **Mr. Nagendra Bandi** explained very clear about basics and involved in practical sessions. This Mentor graphics tool is very easy to understand and we want to learn more about this mentor graphics. So its better to extend this session, practical point of view we have learned so many things. He explained the importance and need of Mentor graphics. Thank you very much to the management and MHRD-IIC for giving the opportunity.