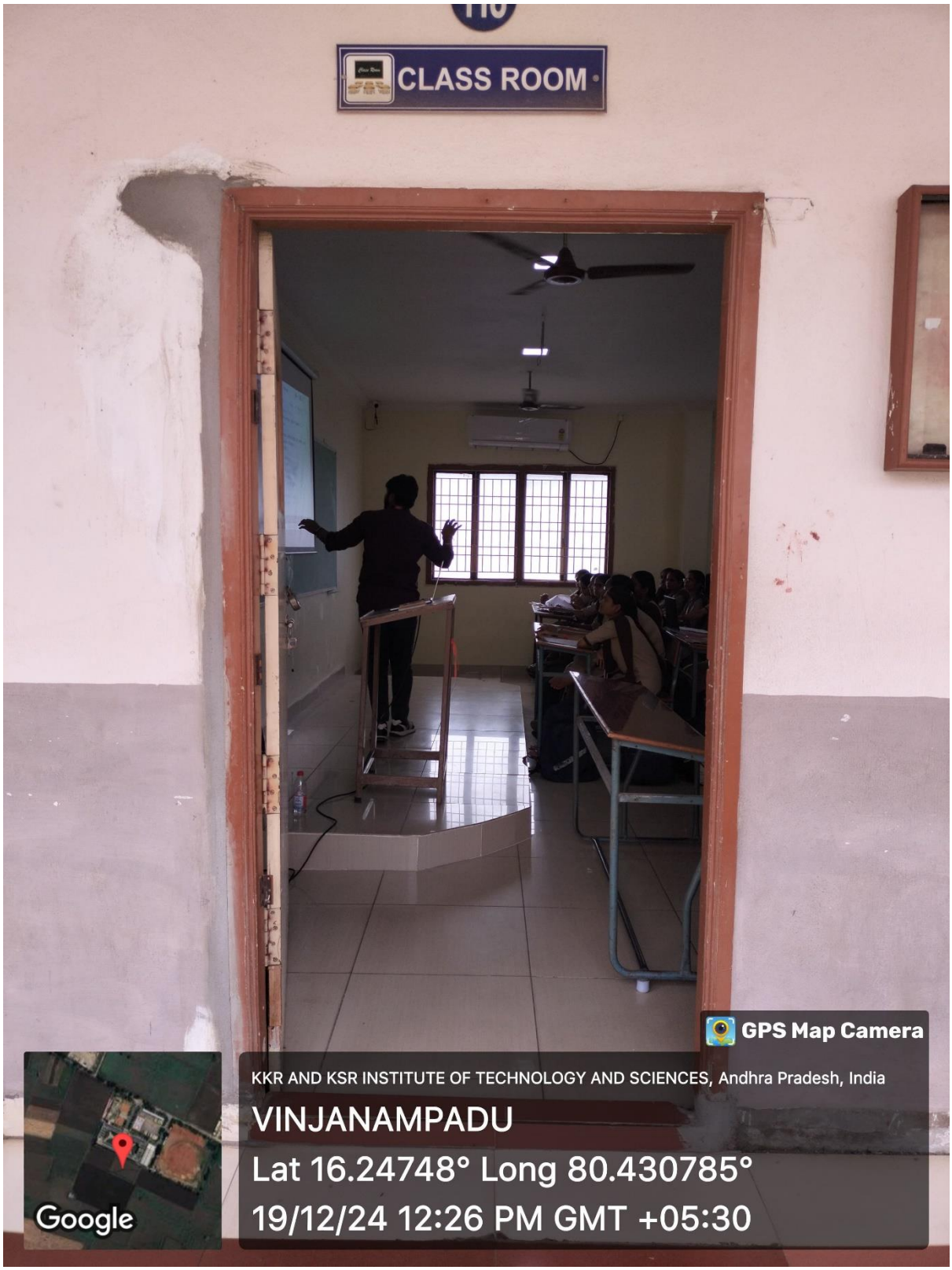
ICT FACILITIES

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Department of Electronics and Communication Engineering

Teaching Slides at a Glance

Signals and Systems

A Signal is an electromagnetic or electrical current that carries data from one system to another system.

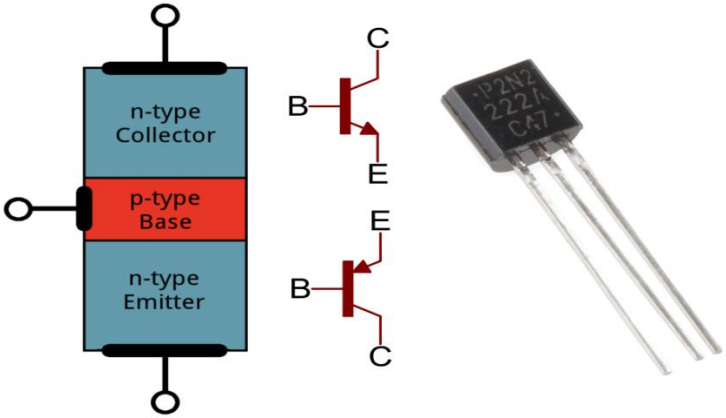
A System is any process that produces an output signal in response to an input signal.

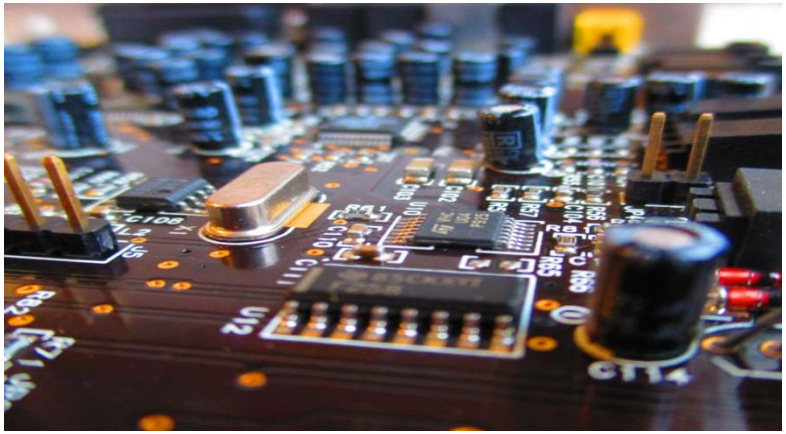
Microprocessor & Microcontroller

A **Microprocessor** is a computer processor where the data processing logic and control is included on a single integrated circuit(IC), or a small number of ICs.

A **Microcontroller** (MCU for microcontroller unit) is a small computer on a single metal-oxide-semiconductor (MOS) integrated circuit chip.

Electronic Devices and Circuits



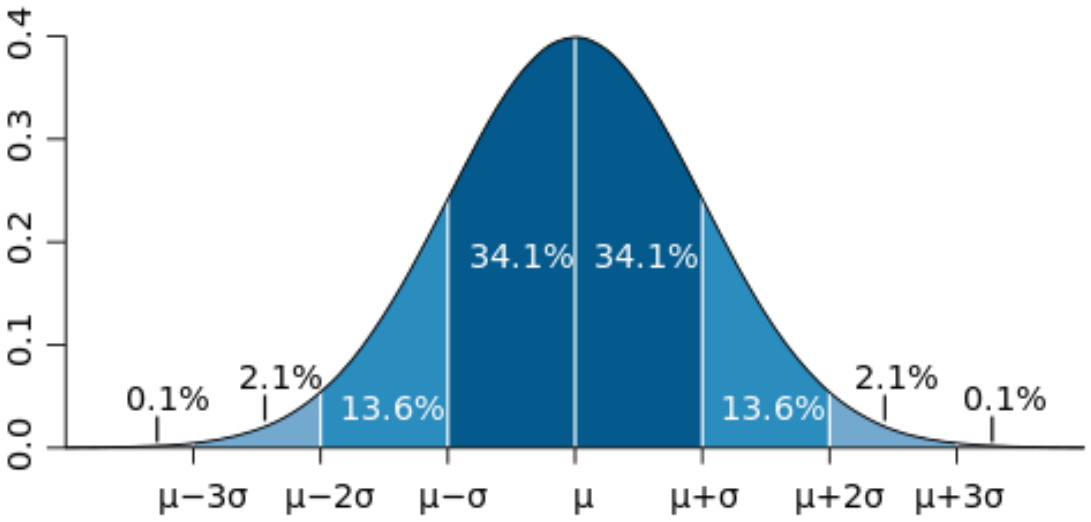


The device which controls the flow of electrons is called electronic device. These devices are the main building blocks of electronic circuits.

One of the most crucial components of an electronic circuit, transistors have revolutionized the field of electronics. These tiny semiconductor devices with three terminals have been around for more than five decades now. They are often used as amplifiers and switchingdevices.

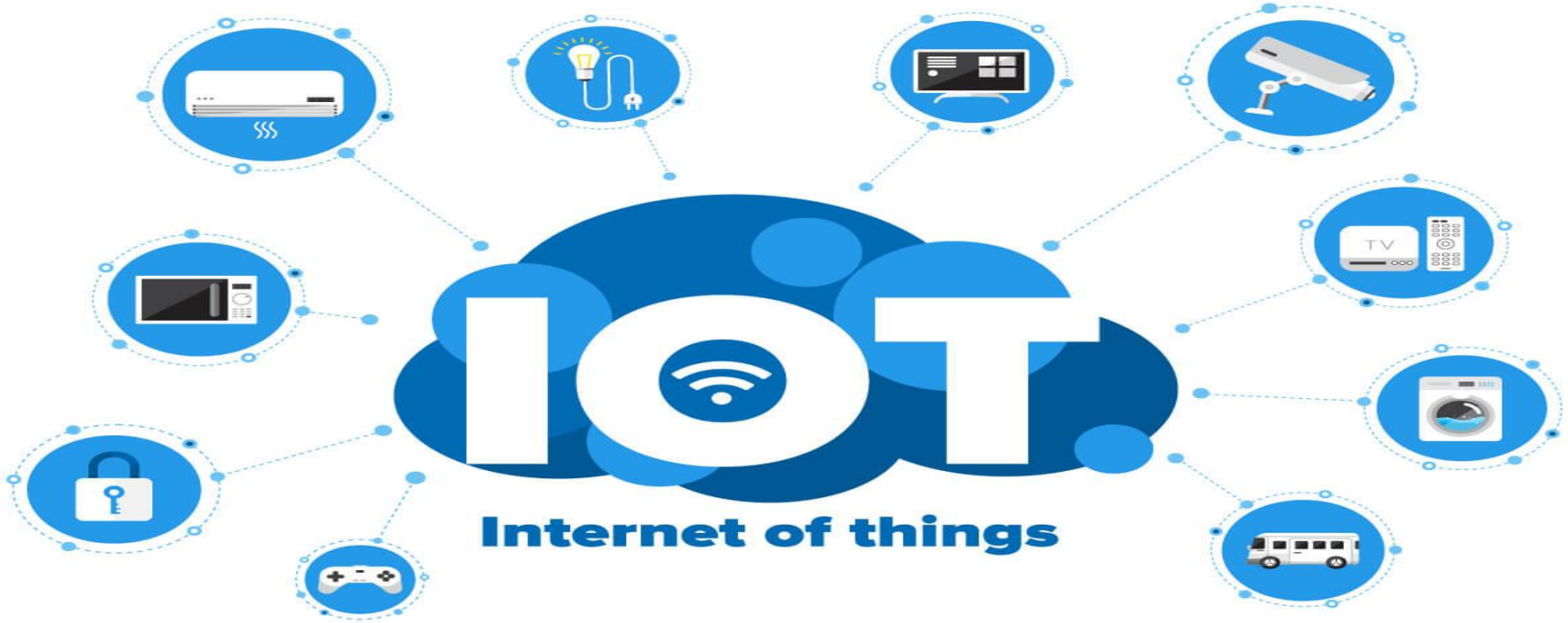
Random Variables and Stochastic Process

A stochastic process, also known as a random process, is a collection of random variables that are indexed by some mathematical set. Each probability and random process are uniquely associated with an element in the set. The index set is the set used to index the random variables.



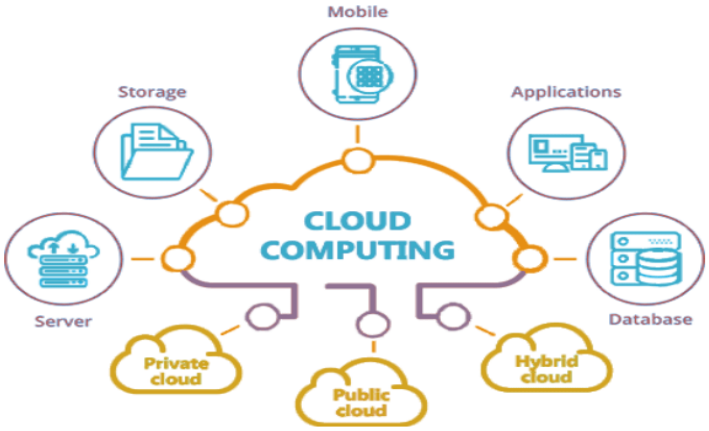
INTERNET OF THINGS

The Internet of things or IoT is a network of interrelated devices and exchange data with other IoT devices and the cloud IoT devices are typically embedded with technology such as sensors and software and can include mechanical and digital machines and consumer objects.



CLOUD COMPUTING

Cloud computing is the on-demand availability of computer system resources, especially data storage (cloud computing) and computing power, without direct active management by the user. Large clouds often have functions distributed over multiple locations, each of which is a data center. Cloud computing relies on sharing of resources to achieve coherence and typically uses a pay-as-you-go model, which can help in reducing capital expenses but also lead to unexpected operating expenses for users.



Field-Programmable Gate Array (FPGA) Design

Definition:

A Field-Programmable Gate Array (FPGA) is an integrated circuit that can be programmed or reprogrammed (capable of being programmed for automatic operation or computer processing) to the required functionality or application after manufacturing.

Characteristics:

Lower complexity

Higher speed

Volume designs and programmable functions.

Advantages

1.Faster time-to-market: No layout, masks or other manufacturing steps are needed for FPGA design. Readymade FPGA is available and burn your HDL code to FPGA.

2. No NRE (Non Recurring Expenses): FPGA tools are cheap.

3. Simpler design cycle: This is due to software that handles much of the routing, placement, and timing.

Manual intervention is less. The FPGA design flow eliminates the complex and time-consuming floor planning, place and route, timing analysis.

4.Field Reprogramability: **A new bit stream (i.e. our program) can be uploaded remotely, instantly. FPGA can be reprogrammed in a snap. FPGA costs start from a couple of dollars to several hundreds or more depending on the hardware features.**

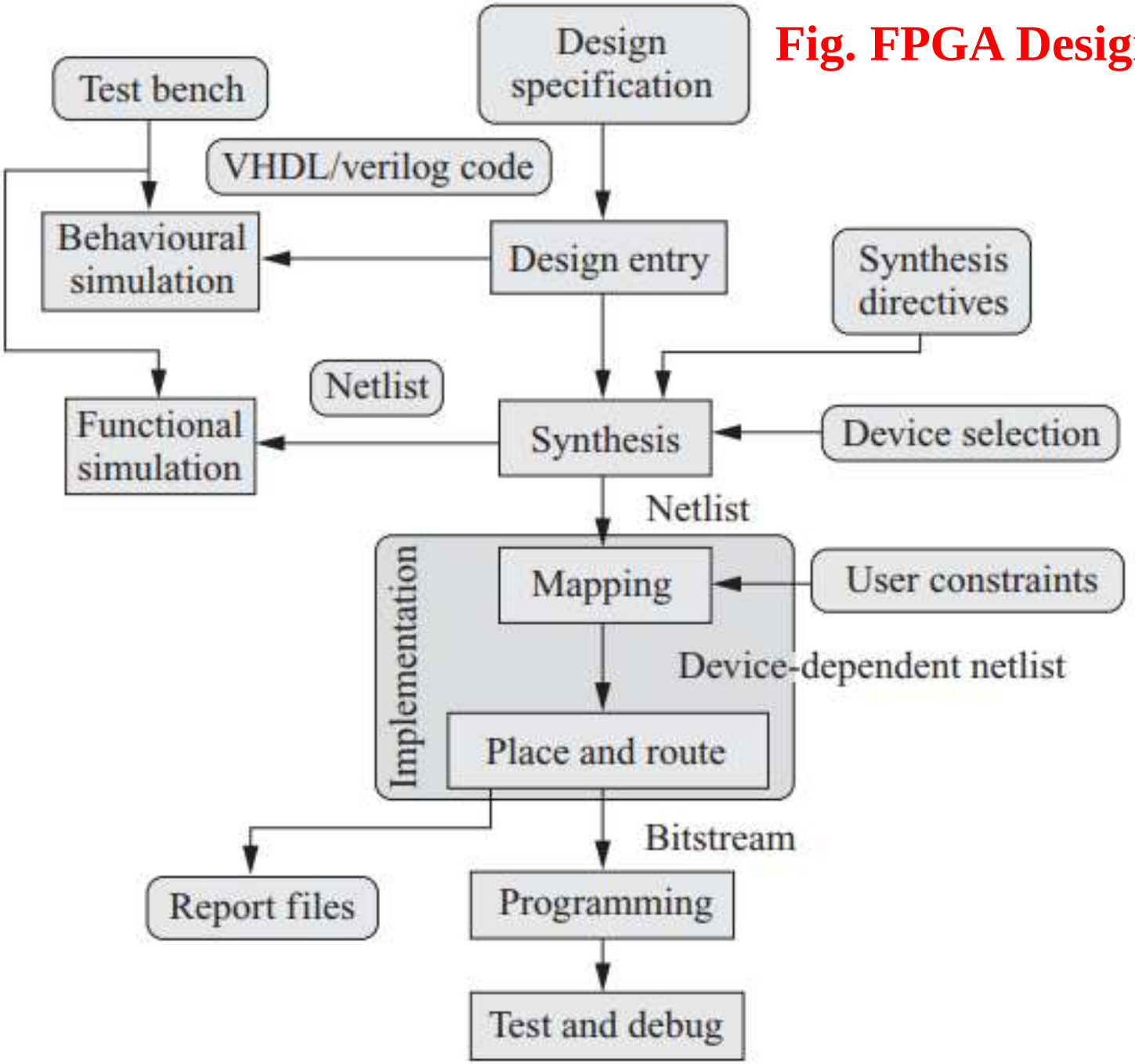
5.Reusability: **Reusability of FPGA is the main advantage.**

Disadvantages:

1. Power consumption in FPGA is more.
2. FPGA limits the design size.
3. Good for low quantity production. As quantity increases cost per product increases.

FPGA Design Flow

Fig. FPGA Design Flow



1. **A typical FPGA Design Flow is shown in Fig.**

2. **The flow starts with the design specifications.**

3. **The functional description of the system is written in a hardware description language (VHDL or Verilog) in the behavioural modeling style.**

4. **The functionality is checked by performing behavioural simulation using a set of test vectors.**

5. **The next step is to perform synthesis. The synthesis step translates the behavioural netlist into a gate level netlist.**

The synthesis step requires the behavioural netlist, the selected device family (e.g., Spartan, Virtex) name, and other synthesis directives.

6.The gate level netlist is again checked for functionality.

7. The user constraints are to be specified for timing, power, etc. Then using the user constraints and gate level netlist, the implementation step is performed.

8. In the implementation step, the mapping of the logic gates are done to the available functional blocks in the FPGA, and the placement and routing are done to complete the implementation.

9.Next, the bit stream file is generated which contains the programming data.

10.The bit stream file is downloaded through the JTAG (Joint Test Action Group) cable into the FPGA device.

11.Downloading the bit stream into the FPGA device is often referred to as FPGA programming.

12.The final step is to test the FPGA device in the system, and debug for any problems in functionality.

Basic FPGA Architecture

A simple FPGA architecture is shown in Fig.

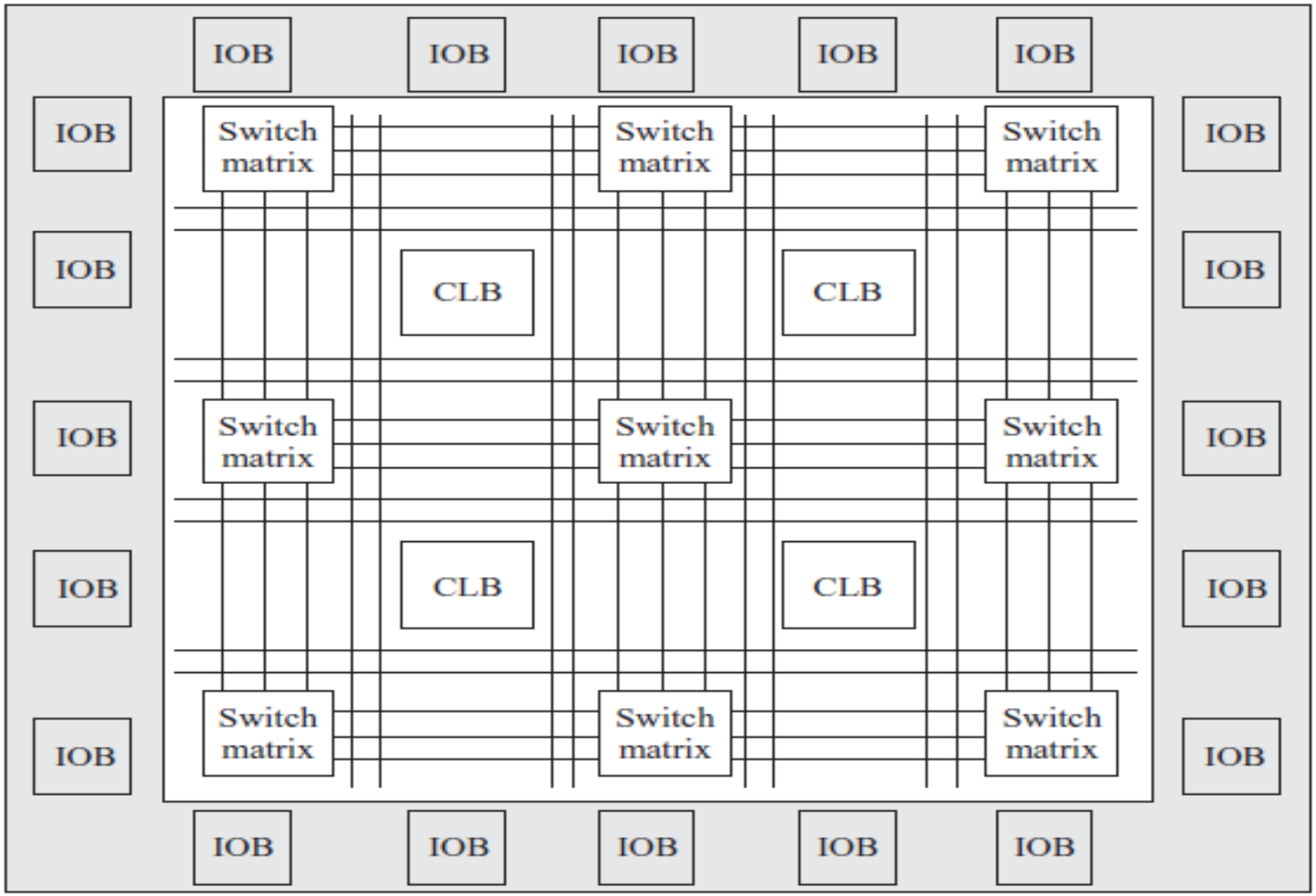


Fig. FPGA Architecture

Basically, it contains four major components; The Configurable Logic Block (CLB), Switch Matrix, Interconnects and the Input Output Block (IOB).

The Configurable Logic Block (CLB):

The Configurable Logic Block (CLB) contains several modules such as lookup tables (LUTs), multiplexers, gates, and flip-flops.

LUT is a combinational logic that stores the truth table of a function. The LUTs are also known as function generators.

The capacity of a LUT is limited by the number of inputs. The advantage of the LUT is that the delay through it is constant.

Switch Matrix:-

The interconnect switch matrix has six switches, which are controlled by the SRAM cell.

Depending on the bit stored in the SRAM cell, the connection is established between the horizontal and the vertical interconnect wires.

Interconnects:-

Interconnects arranged in horizontal and vertical channels.

Each channel contains some number of short, long, and very long wires. The short wire segments span a single CLB, the long segments span two CLBs,

and very long segments span the entire length or width of the chip.

Input/Output Block:- used for outside world to communicate in applications.

FPGA Programming Technologies

1.Antifuse-based FPGA

2.EPROM-based FPGA

3. SRAM-based FPGA

Antifuse-based FPGA:-

- **The antifuse FPGAs are programmed by applying high voltage between the two terminals of the fuse to break down the dielectric material of the fuse.**

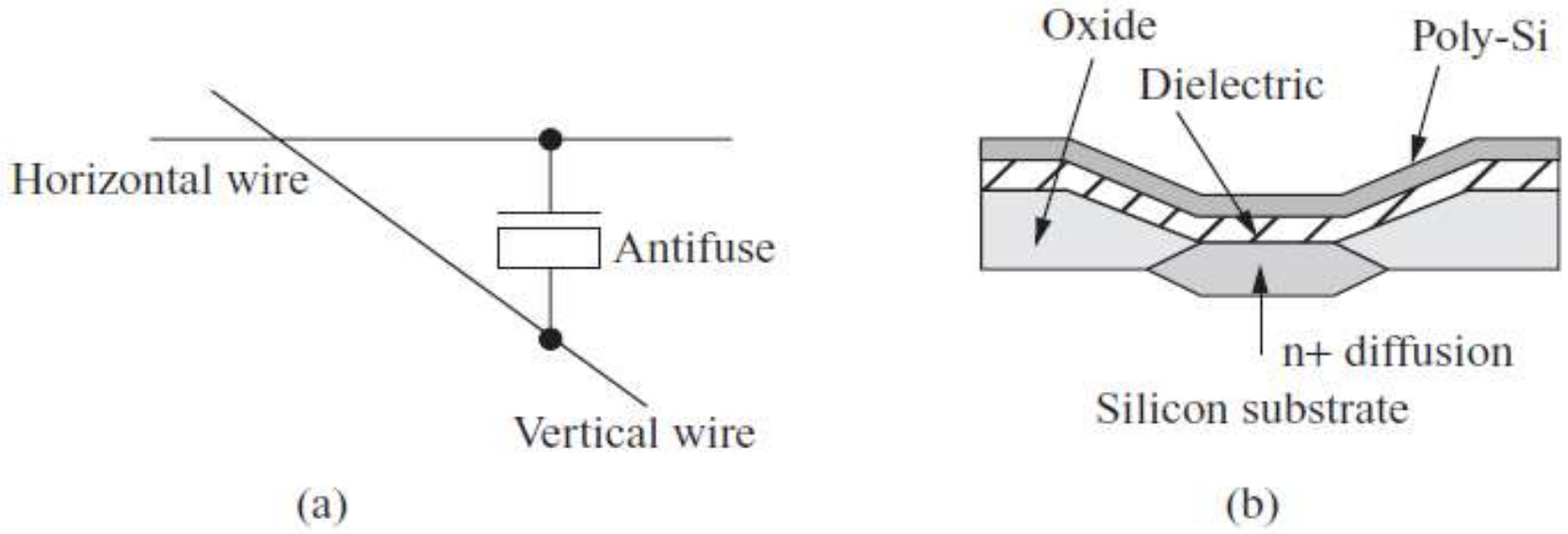


Fig. Antifuse switch used in FPGA (a) schematic (b) structure

➢**The antifuse switch used in FPGA is shown in Fig. Antifuse structure is normally used in an open circuit condition. However, when they are programmed, a low resistance path is established.**

➢**As shown in Fig., the top and bottom layers are conducting, and the middle layer is an insulator. In normal conditions, the insulating layer isolates the top and bottom layers.**

➢**When the antifuse is programmed, a low resistance path is established through the insulator. The antifuse switches have smaller on-resistance and parasitic capacitance than pass transistors and transmission gates.**

- **Hence, it supports higher switching speed. Antifuse switches are one-time programmable, so design changes are not possible.**

EPROM based FPGA:- **The FPGAs use EPROM and EEPROM technology which are programmed using high voltages.**

The devices are reprogrammable and nonvolatile, and can be programmed while the devices are embedded in the system.

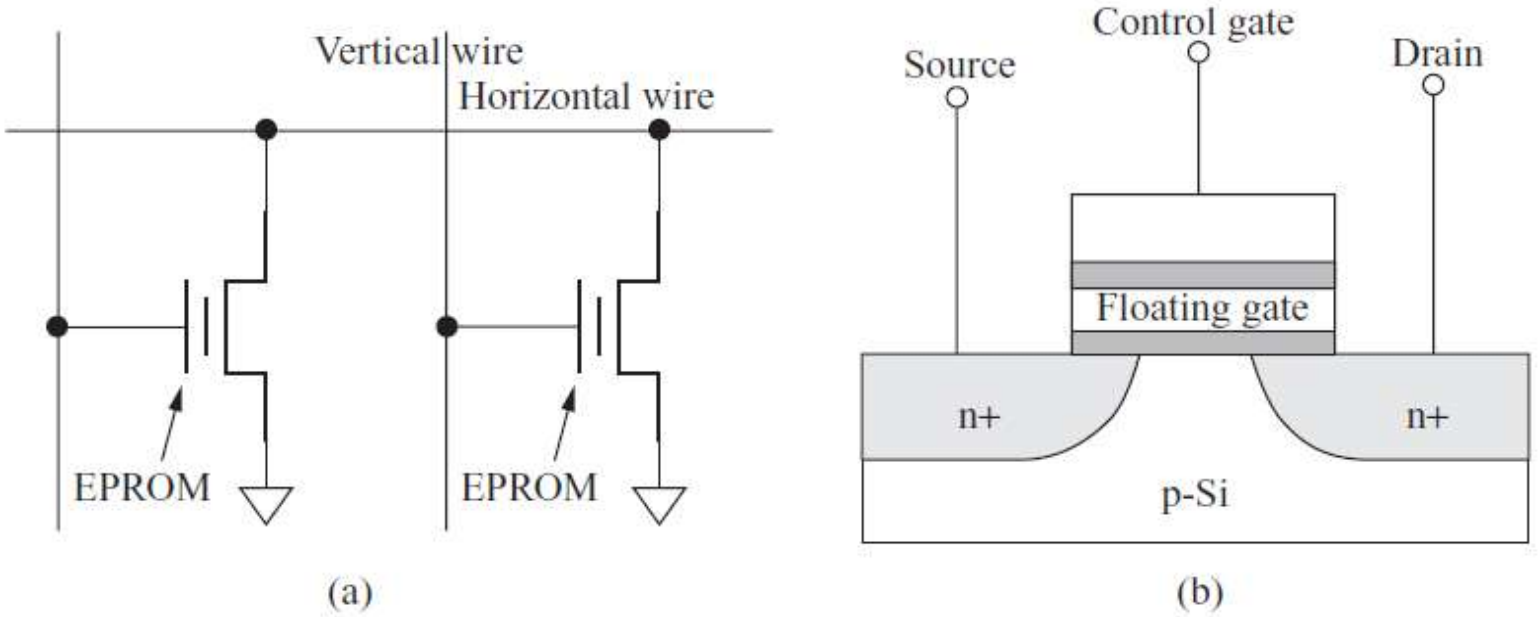


Fig. (a) Switch interconnection (b) EPROM (flash) memory cell

The EPROM and EEPROM programming is based on the flash memory cell as shown in Fig. which uses two gates, one is the control gate and another is the floating gate.

Under normal mode of operation, there are no changes on the floating gate, and the transistor behaves like a normal transistor with low threshold voltage.

When a high voltage is applied to the control gate, the floating gate is charged, and the threshold voltage is increased. The transistor becomes permanently OFF.

SRAM-based FPGA :- In the SRAM-based FPGA, the logic functions are based on the stored bits in the SRAM. These devices use CMOS transmission gates for switching.

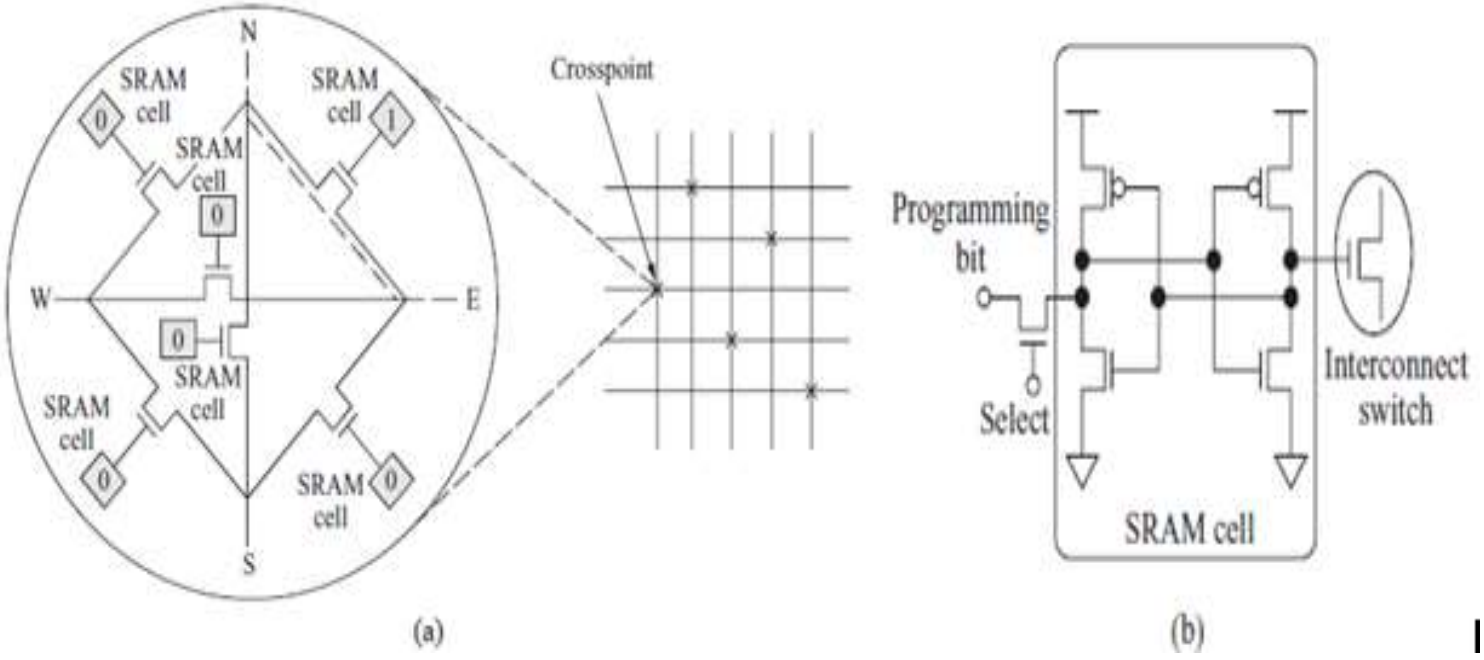


Fig. SRAM-based crosspoint switch matrix (a) crosspoint switch (b) SRAM cell

The interconnect switch matix is shown in Fig. (a). Each crosspoint has six switches, which are controlled by the SRAM.

Depending on the bit stored in the SRAM, the connection is established between the horizontal and the vertical interconnect wires.

For example, in Fig. (a), the north-to-east (NE) connection is established by the SRAM containing a bit 1. This makes the nMOS transistor ON, and the connection between N and E is established.

The internal circuit diagram of a SRAM cell is shown in Fig. (b).

FPGA Families

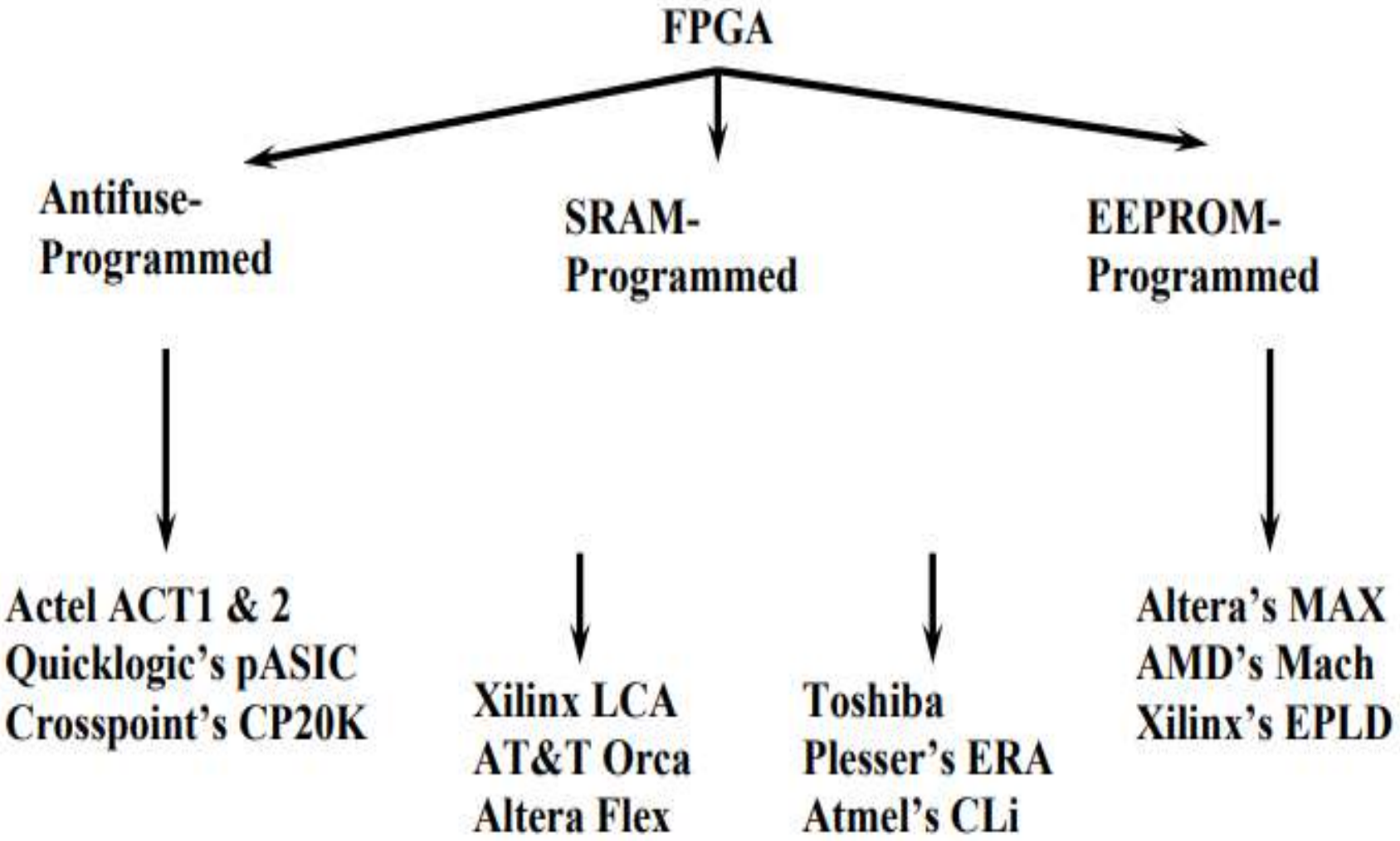
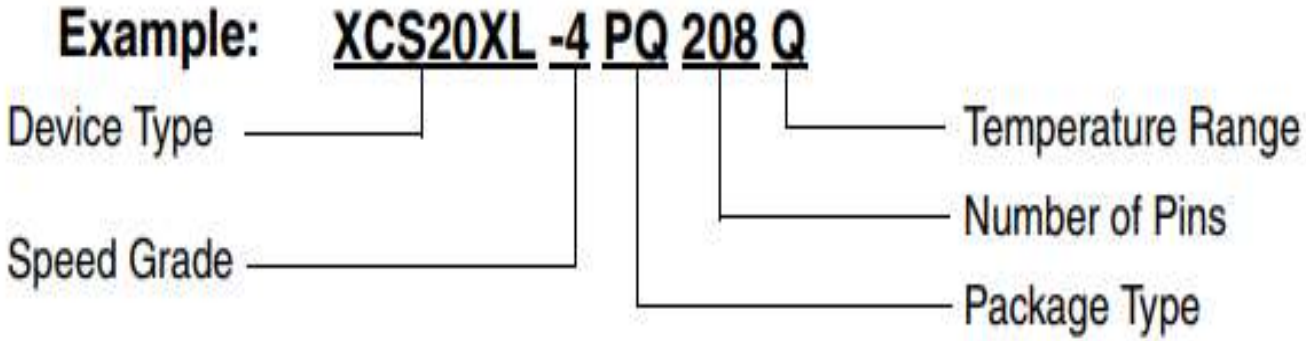
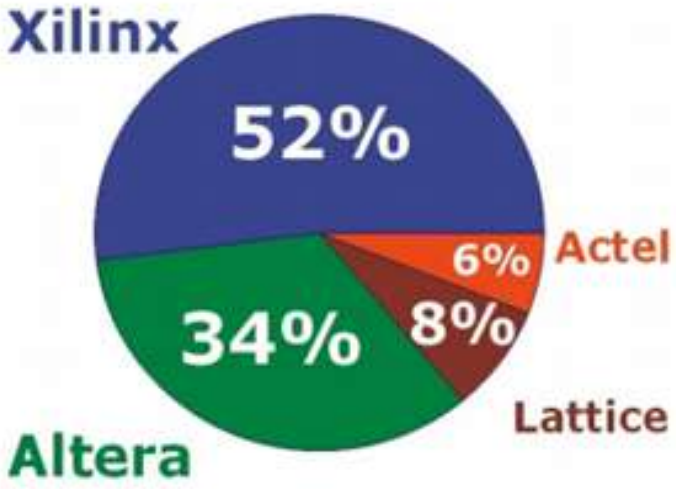


Fig. FPGA Classification on user Programmable Technologies

Ordering Information





Altera Flex 8000FPGA

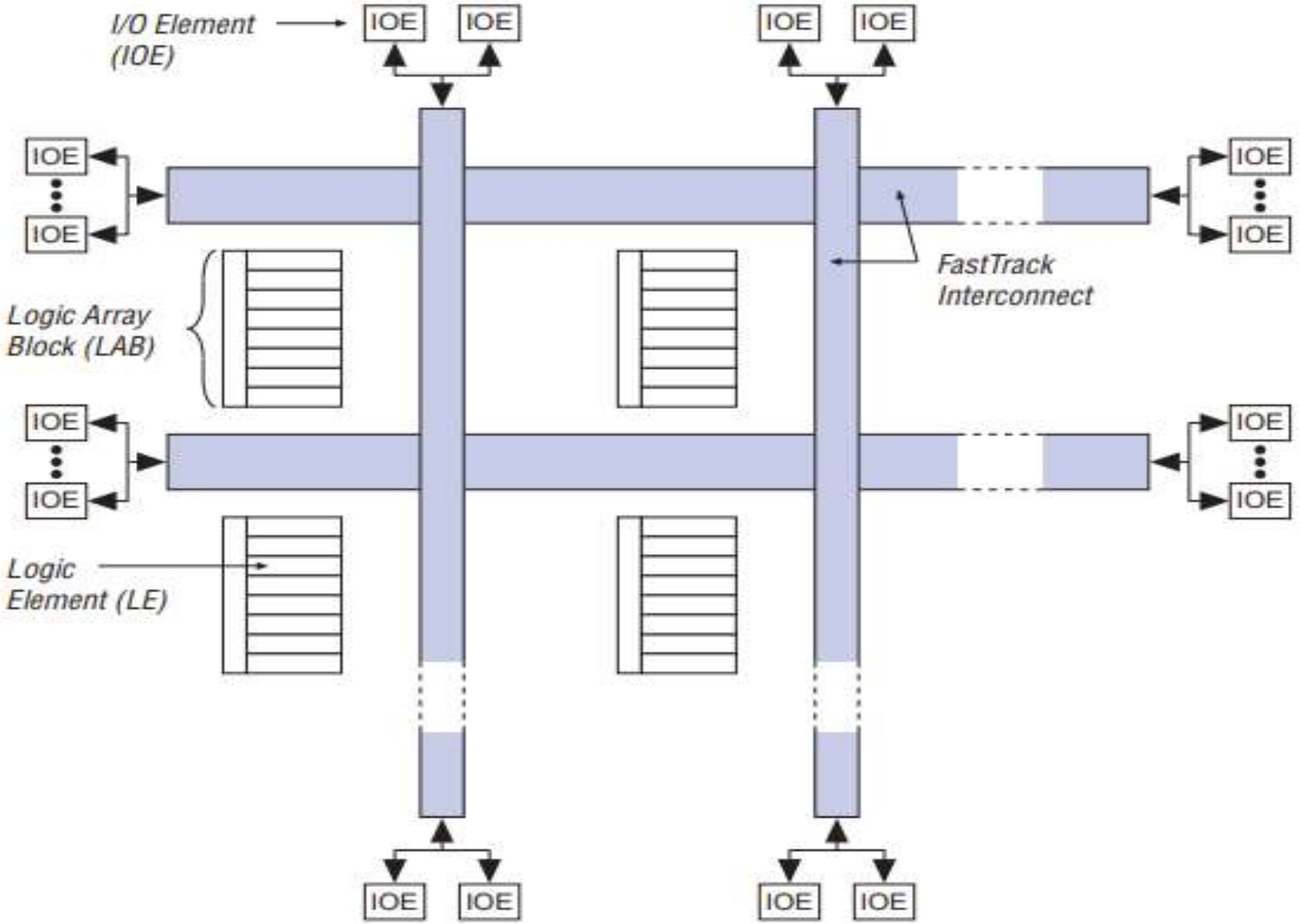


Fig. Altera FLEX 8000FPGA Block Diagram

The Block Diagram of Altera FLEX 8000FPGA is shown in Fig.

1. Logic Array Block **2. Logic Element**

3. Carry Chain **4. Cascade Chain**

5. Input/output Element **6. Operating Modes**

1. Logic Array Block:

Altera FLEX 8000 chip contains 26-162 Logic Array Blocks (LABs).

Each LAB contains 8 Logic Elements (LEs), so a chip contains 208–1296 LEs, totaling 2,500–16,000 usable gates, plus local interconnect, control signals, carry & cascade chains.

LABs arranged in rows and columns, connected by Fast Track Interconnect, with I/O elements (IOEs) at the edges.

2.Logic Element: Each LE contains 4-input Look-Up Table (LUT) can produce any function of 4 variables and programmable flip-flops.

3.Carry Chain: It provides very fast (< 1ns) carry-forward between LEs (Good for high-speed adders & counters).

4.Cascade Chain: It provides **wide fan-in**

5.Input/output Element: **Eight I/O Elements (IOEs) are at the end of each row and column can be used as either input, output or bidirectional pins.**

6.Operating Modes: **Altera FLEX 8000FPGA contains three operating modes.**

They are Normal mode (used for general logic applications) Arithmetic mode Provides (to implement adders, accumulators, and comparators) Up/down counter mode (Provides counter enable, synchronous up/down control and data loading options).

Features of Altera FLEX 8000FPGA

Low-cost, high-density, register-rich CMOS programmable logic device (PLD) family.

In-circuit reconfigurability.

Low power consumption.

Built-in Joint Test Action Group (JTAG) and boundary-scan test (BST) circuitry compliant with IEEE Std. 1149.1-1990 on selected devices.

Flexible interconnect.

Powerful I/O pins.

Altera Flex 10K FPGA

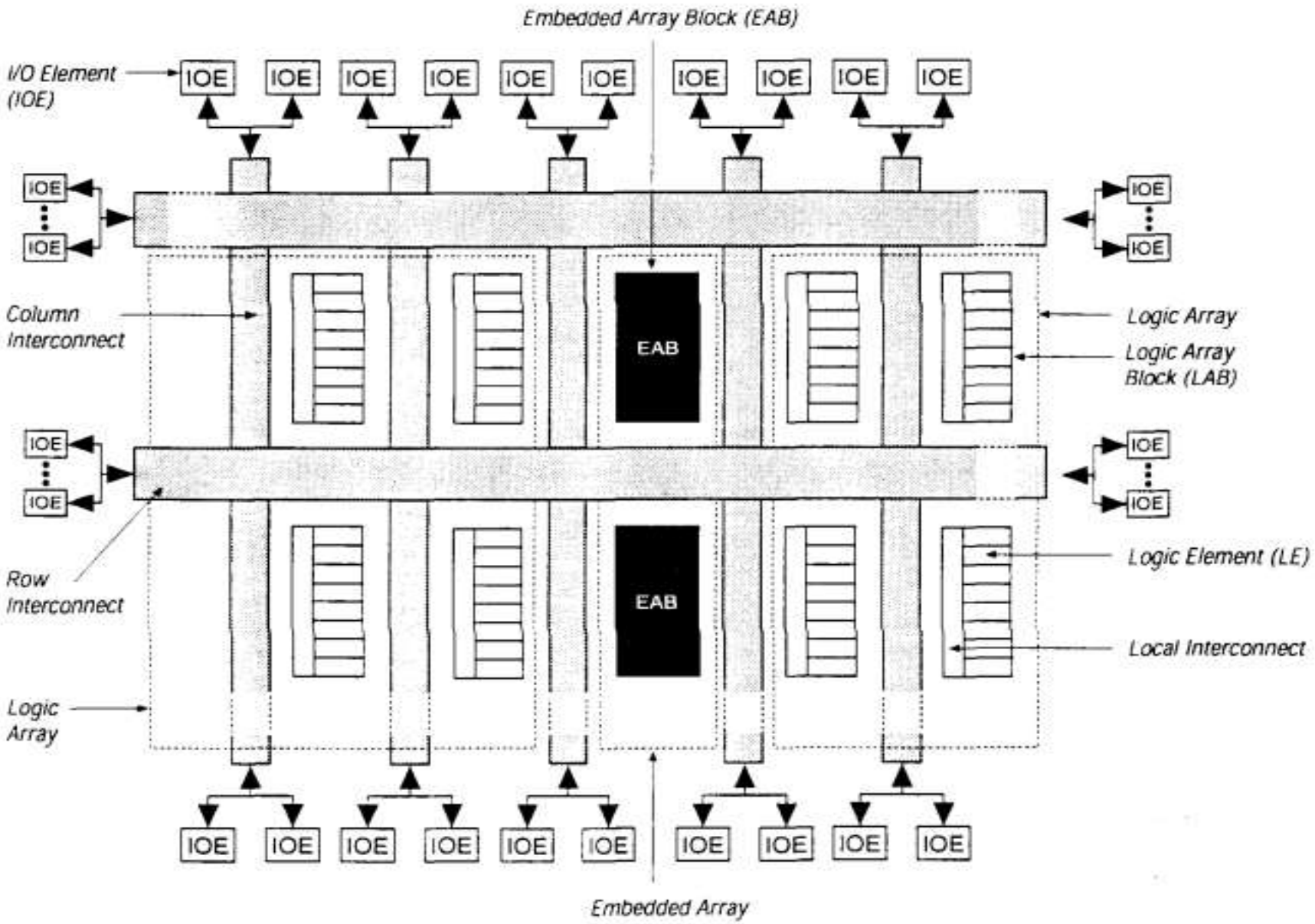


Fig. 8 Altera FLEX 10K FPGA Block Diagram

The Block Diagram of Altera FLEX 10K FPGA is shown in Fig.

Altera FLEX 10K chip contains 72–1520 Logic Array Blocks (LABs).

Each LAB contains 8 Logic Elements (LEs), so a chip contains 576–12,160 LEs, totaling 10,000–250,000 usable gates.

Each chip also contains 3–20 Embedded Array Blocks (EABs), used to implement either logic or memory.

When used to implement logic, an EAB can provide 100 to 600 gate equivalents and used to create complex logic functions such as multipliers, microcontrollers, large state machines and Digital Signal Processing.

Each EAB can be used independently or combined to implement larger functions.

Using EABs to implement memory, a chip can have 6K–40K bits of RAM.

Each EAB provides 2,048 bits of RAM, plus input and output registers, can be used to implement synchronous RAM, ROM, dual-port RAM, or FIFO.

The Altera FLEX 10K families feature the largest device in the programmable logic industry.

With higher density and higher performance, the Altera Flex 10K device family offers a faster and more efficient design solution than other FPGAs.

Xilinx XC4000 series FPGA

In 1985, Xilinx introduced the first FPGA family, called the XC2000 series. Now they have many versions such as XC3000, XC4000, XC5000, Spartan, and Virtex series.

Xilinx has recently introduced an FPGA family based on antifuses, called the XC8100.

The Xilinx 4000 family devices range in capacity from about 2000 to more than 15,000 equivalent gates.

The Simplified Block Diagram of XC4000 series FPGA Configurable Logic Block is shown in Fig.

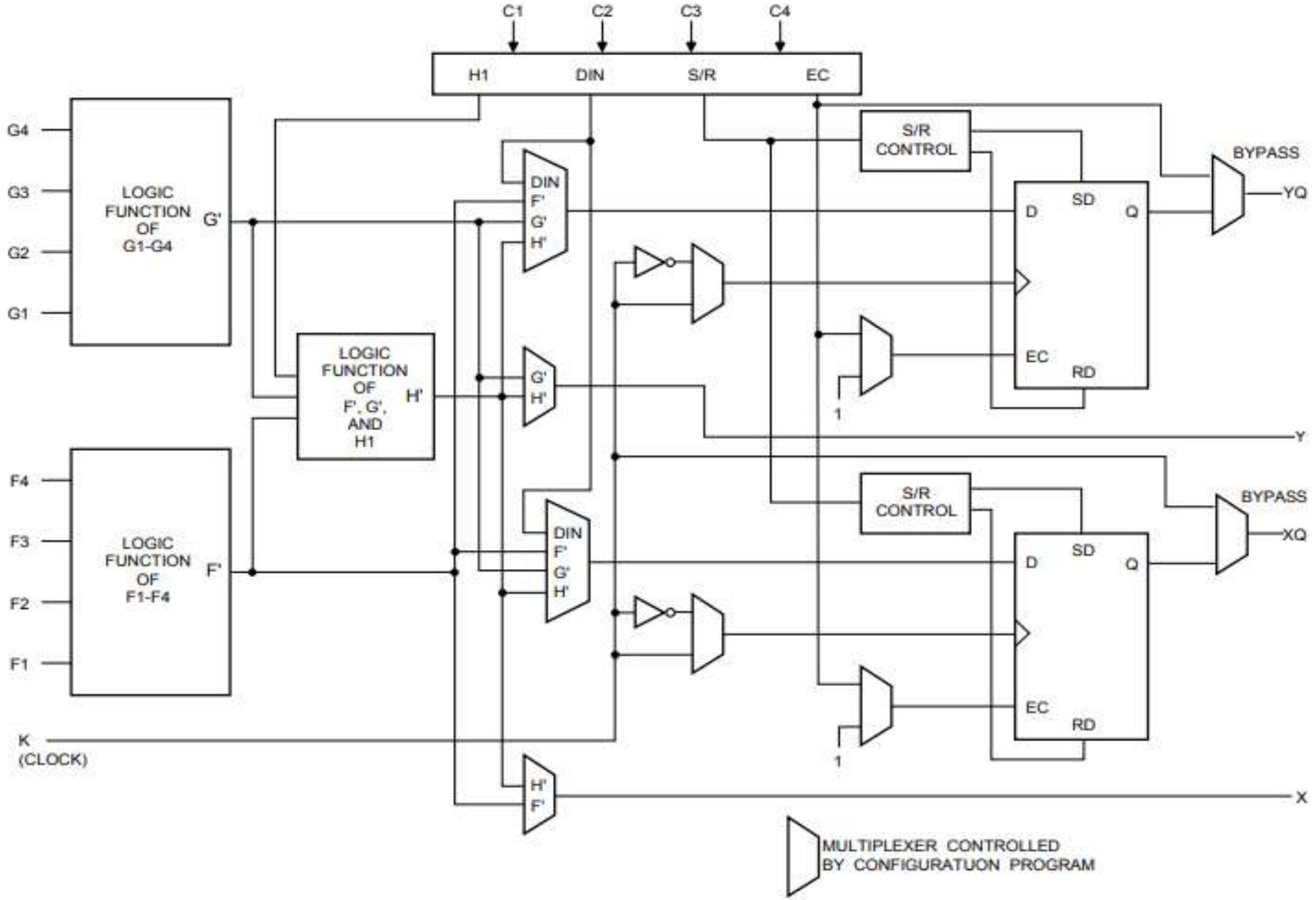


Fig. Simplified Block Diagram of XC4000 series FPGA Configurable Logic Block

The XC4000 consists of a Configurable Logic Block (CLB) that is based on Look-Up-Tables (LUTs).

A LUT with *n* inputs can realize any logic function with *n* inputs by programming the logic function's truth table directly into the memory.

CLBs provide the functional elements for constructing the user's logic.

The XC4000 CLB contains three separate LUTs, as shown in Fig. There are two 4-input LUTs that are fed by CLB inputs, and the third LUT is used in combination with the other two LUTs.

This arrangement allows the CLB to implement a wide range of logic functions of up to nine inputs, two separate functions of four inputs, or other possibilities. Each CLB also contains two flip-flops.

Multiplexers in the CLB map the four control inputs (C1 - C4) into the four internal control signals (H1, DIN, S/R and EC). Any of these inputs can drive any of the four internal control signals.

EC - Enable Clock,

SR/H0 - Asynchronous Set/Reset or H function generator Input 0,

DIN/H2 - Direct In or H function generator Input 2
and
H1 - H function generator Input 1.

The two storage elements in the CLB are edge-triggered D-type flip-flops with common clock (K) and clock enable (EC) inputs.

A third common input (S/R) can be programmed as either an asynchronous set or reset signal independently for each of the two registers.

Each flip-flop can be triggered on either the rising or falling clock edge.

The source of a flip-flop data input is programmable: it is driven either by the functions F', G' and H' or the Direct In (DIN) block input. The flip-flops drive the XQ and YQCLB outputs.

In addition, each CLB F' and G' function generator contains dedicated arithmetic logic for the fast generation of carry and borrow signals, greatly increasing the efficiency and performance of adders, sub tractors, accumulators, comparators and even counters.

Xilinx Spartan XL FPGA

Spartan series devices achieve high-performance, low-cost operation through the use of an advanced architecture and semiconductor technology.

Spartan series FPGAs can be used where hardware must be adapted to different user applications.

Spartan series FPGAs are implemented with a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a powerful hierarchy of versatile routing resources (routing channels) and surrounded by a perimeter of programmable Input/Output Blocks (IOBs) as seen in Fig.

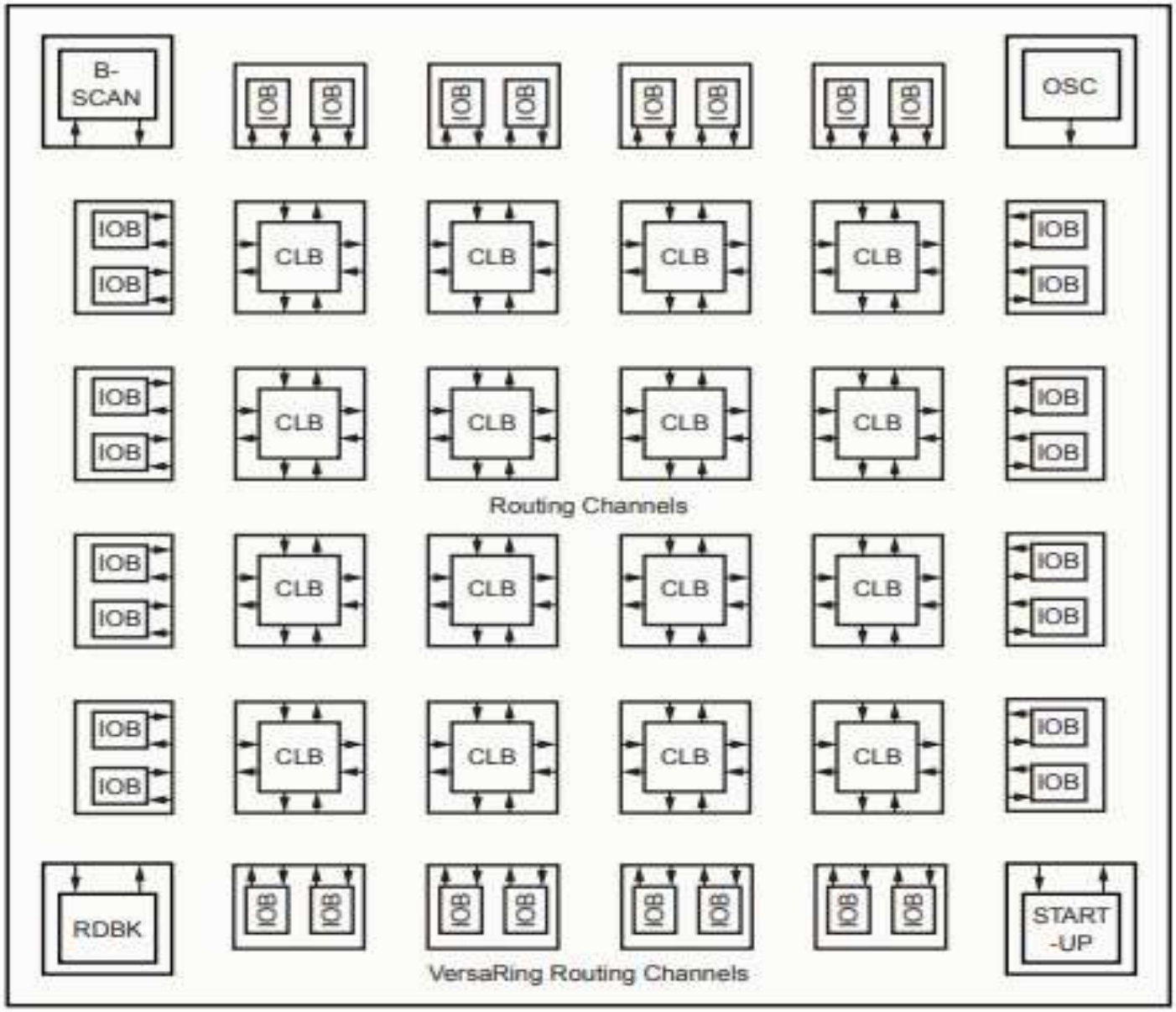


Fig. Basic Xilinx Spartan XL FPGA Block Diagram

Device	Logic Cells	Max System Gates	Typical Gate Range (Logic and RAM)(1)	CLB Matrix	Total CLBs	No. of Flip-flops	Max. Avail. User I/O	Total Distributed RAM Bits
XCS05 and XCS05XL	238	5,000	2,000-5,000	10 x 10	100	360	77	3,200

CLBs provide the functional elements for implementing the user's logic.

Each CLB contains two flip-flops that can be used to register (store) the function generator outputs.

The functionality of each circuit block is customized during configuration by programming internal static memory cells.

The values stored in these memory cells determine the logic functions and interconnections implemented in the FPGA.

IOBs provide the interface between the package pins and internal signal lines.

Routing channels provide paths to interconnect the inputs and outputs of the CLBs and IOBs.

All internal routing channels are composed of metal segments with programmable switching points and switching matrices to implement the desired routing.

A structured, hierarchical matrix of routing channels is provided to achieve efficient automated routing.

The CLB routing channels which run along each row and column of the CLB array. IOB routing channels which form a ring (called a VersaRing) around the outside of the CLB array. It connects the I/O with the CLB routing channels.

The routing channels around the CLB are derived from three types of interconnects; single-length, double-length, and long lines. At the intersection of each vertical and horizontal routing channel is a signal steering matrix called a Programmable Switch Matrix (PSM).

Two 16 x 1 memory look-up tables (F-LUT and G-LUT) are used to implement 4-input function generators. A third 3-input function generator (H-LUT) can implement any Boolean function of its three inputs.

The IEEE Boundary Scan Standard 1149.1 was developed to facilitate board-level testing of electronic assemblies. Design and test engineers can embed a standard test logic structure in their device to achieve high fault coverage for I/O and internal logic.

Xilinx Spartan II FPGA

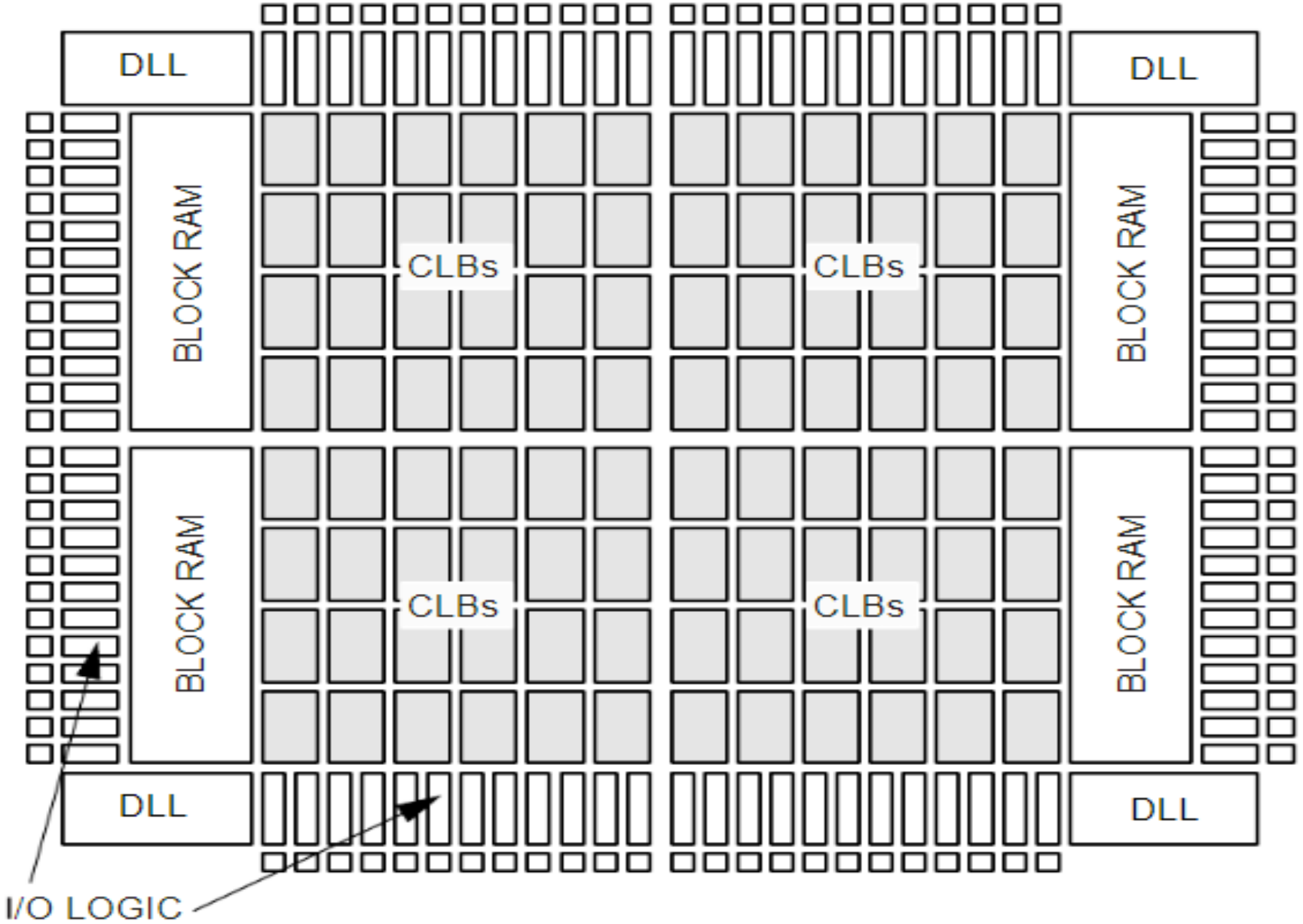


Fig. Basic Spartan-II Family FPGA Block Diagram

Device	Logic Cells	System Gates (Logic and RAM)	CLB Array (R x C)	Total CLBs	Maximum Available User I/O(1)	Total Distributed RAM Bits	Total Block RAM Bits
XC2S15	432	15,000	8 x 12	96	86	6,144	16K

The Spartan-II family of FPGAs have a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), surrounded by a perimeter of programmable Input/output Blocks (IOBs) as shown in Fig.

There are four Delay-Locked Loops (DLLs), one at each corner of the die. Two columns of block RAM lie on opposite sides of the die, between the CLBs and the IOB columns.

Configurable Logic Block (CLB)

CLB is the basic building block of the Spartan-II FPGA. ACLB includes a 4-input function generator, carry logic and storage element.

Block Ram

Block RAM memory blocks are organized in columns. All Spartan-II devices contain two such columns, one along each vertical edge. These columns extend the full height of the chip.

Delay-Locked Loop (DLL)

Associated with each global clock input buffer is a fully digital Delay- Locked Loop (DLL) that can eliminate skew between the clock input pad and internal clock-input pins throughout the device. Each DLL can drive two global clock networks. The DLL monitors the input clock and the distributed clock and automatically adjusts a clock delay element.

Input/Output Block

The Spartan-II FPGA IOB supports a wide variety of I/O signaling standards. These high-speed inputs and outputs are capable of supporting various state of the art memory and bus interfaces.

The three IOB registers function either as edge-triggered D-type flip-flops or as level-sensitive latches.

Each IOB has a clock signal (CLK) shared by the three registers and independent Clock Enable (CE) signals for each register.

In addition to the CLK and CE control signals, the three registers share a Set/Reset (SR).

Xilinx Virtex FPGA

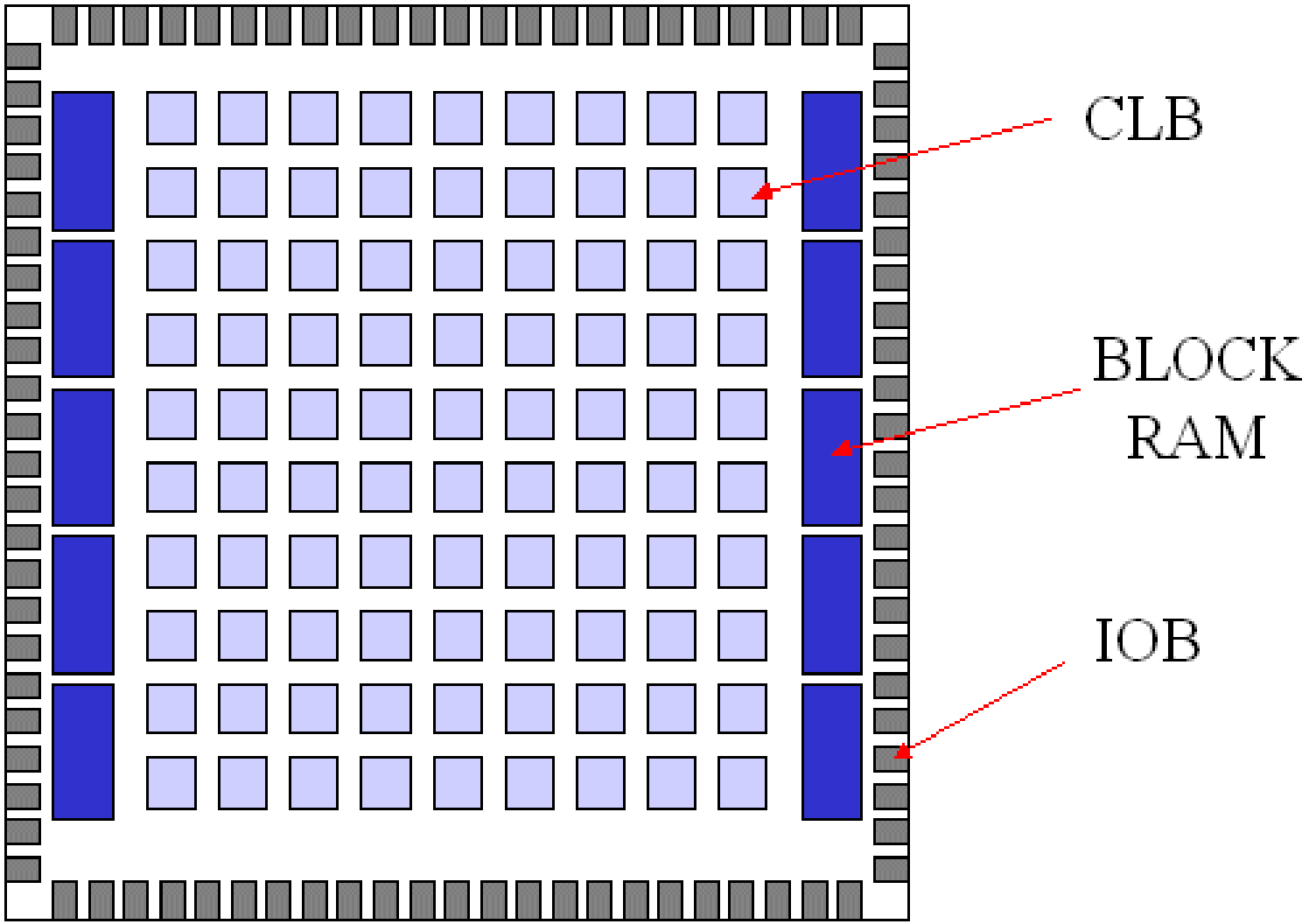


Fig. 12 Xilinx Virtex FPGA Architecture Overview

Virtex FPGAs are composed of an array of Configurable Logic Blocks (CLBs) surrounded by a ring of Input/Outputs Blocks (IOBs). On the east and west edges are Block RAMs (BRAMs).

The CLBs are the primary building blocks that contain elements for implementing customizable gates, flip flops, and wiring for connectivity.

The **IOBs** provide circuitry for communicating signals with external devices. The general routing uses two kinds of wires: singles and hex's.

Signal terminate at an adjacent CLB, while Hex's terminate at CLBs 6 positions over. Singles should be used to transport data between local CLBs, whereas Hex's should be used to transport data to non-local CLBs.

The BRAMs allow for synchronous or asynchronous storage of kilobits of data, though each CLB can also implement synchronous/asynchronous 32-bit RAMs.

Internal Architecture of Virtex CLB:-

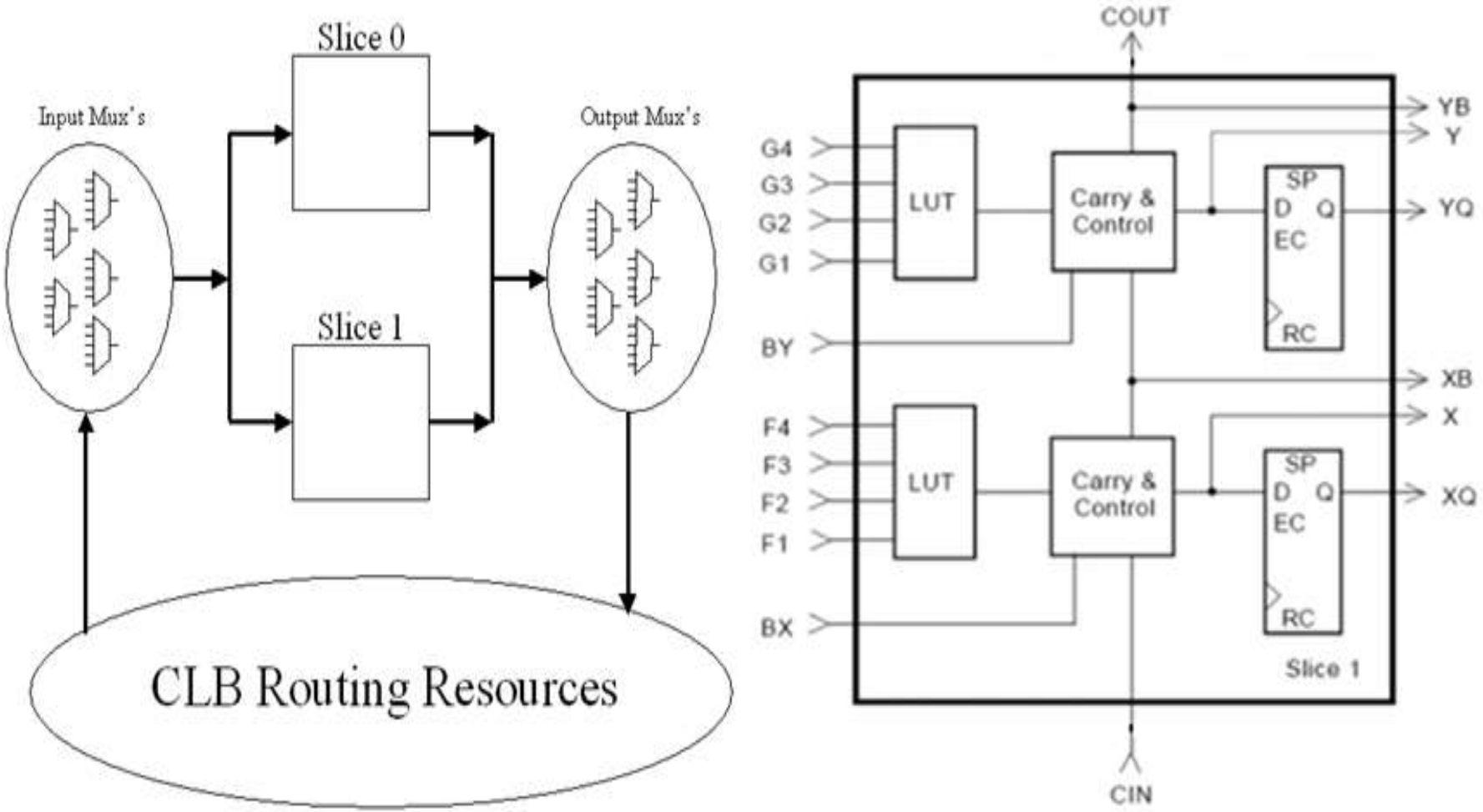


Fig. (a)Xilinx Virtex CLB overview and (b) internal overview of Slice.

Each CLB contains two slices. Each slice implements two 4-input Look-Up-Tables (LUTs), 2 D-Type flip-flops, and some carry logic.

A Virtex slice is similar in functionality to a Xilinx XC4000 CLB, which means that each Virtex CLB has roughly twice the logic capacity of a XC4000 CLB.

The general routing allows data to be passed to or received from other CLBs.

The input mux's allow wires in the general routing to pass data to the slices, while the output mux's allow the slices to pass data to wires in the general routing.

The primary elements in the slices are the F and G LUTs, and the X and Y flip flops. The LUTs can be used to implement gates or to implement small memories. The flip flops can be used to create state machines.

The slices also have internal mux's to control the connectivity of internal resources. Finally, there is logic inside each slice to implement fast carries for arithmetic type logic.