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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VLSI Design

Course Outcomes

Faculty Name: A. Sarath Kumar /J. Sairam **A.Y:** 2023-24

Name of the Course: VLSI Design

Subject Code : 20EC6T03 **Class:** III Year II SEM

CO code	CO Description	Taxonomy Level
C322.1	Understand various fabrication steps and electrical properties of MOS circuits	Understand
C322.2	Outline the Stick & Layout Diagrams for MOS circuits	Understand
C322.3	Demonstrate the basic circuit concepts & Scaling models to the MOS transistors	Apply
C322.4	Identify various Static and dynamic CMOS circuit designs	Apply
C322.5	Illustrate various FPGA architectures and Advanced IC's	Understand

Course Outcomes Mapping with PO's and PSO's

CO-PO Mapping

CO code	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
C322.1	3		2									
C322.2	3	2										
C322.3		3	3									
C322.4	3	2			3							
C322.5		3	3									
Average	**3**	**3**	**3**		**3**							

CO-PSO Mapping

CO code	PSO1	PSO2	PSO3	PSO4
C322.1	3	2	3	2
C322.2	2	3	2	2
C322.3	3	2	2	2
C322.4		3	2	2
C322.5		2	2	3
Average	3	2	2	2

CO-PO Mapping Justification

MAPPING	CORRELATION LEVELS	MAPPING REASONS
C322.1-PO1	3	To understand the fabrication steps and technology basic knowledge of Engineering is needed
C322.1-PO3	2	The designed structures provide solutions for complex real time problems
C322.2-PO1	3	For drawing stick diagram basic knowledge is needed
C322.2-PO2	2	Design of stick diagrams is by analyzing the complex problems and to provide simple representation
C322.3-PO2	3	Circuit concepts and scaling needs the concept of problems analysis
C322.3-PO3	3	With the concept of scaling appropriate miniaturization can be obtained
C322.4-PO1	3	For the static and dynamic analysis mathematical and physical insight is needed
C322.4-PO2	2	Study of static and dynamic analysis provides solution for complex problems
C322.4-PO5	3	To makes the analysis modern tool should be utilized
C322.5-PO2	3	To understand and design the FPGA survey on existing literature is essential to develop optimal solution.
C322.5-PO3	3	Design of FPGA provides the solution for existing problems

CO-PSO Mapping justification

MAPPING	CORRELATION LEVELS	MAPPING REASONS
C322.1-PSO1	3	Fabrication requires application if VLSI knowledge
C322.1-PSO2	2	This provides solution for design of digital system
C322.1-PSO3	3	For designing VHDL programming skills are required
C322.1-PSO4	2	This will be basic requirement for analysis of future research trends in VLSI
C322.2-PSO1	2	For design of stick diagrams knowledge of VLSI steps are required
C322.2-PSO2	3	This is direct solution for design of IC's
C322.2-PSO3	2	For various conversions such as net list programming skills are required
C322.2-PSO4	2	While designing new trends are to be considered
C322.3-PSO1	3	Scaling is possible if we possess knowledge on fabrication
C322.3-PSO2	2	This is one of the much-needed technique for miniaturization
C322.3-PSO3	2	For validation and initial testing software skills are required
C322.3-PSO4	2	Scaling always gives scope of new trends in research and development
C322.4-PSO2	3	Static and dynamic characteristics are needed for providing new solutions
C322.4-PSO3	2	Analysis can be performed by using software tools
C322.4-PSO4	2	Analysis of circuits and new trends is always new field of research
C322.5-PSO2	2	FPGA design aspects provides solution for many issues
C322.5-PSO3	2	For design and analysis of FPGA software skills are required
C322.5-PSO4	3	Design aspects of FPGA is current state of art research

Signature of the faculty

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DEPARTMENT OF ECE (ELECTRONICS AND COMMUNICATION ENGG)

Name of the Faculty: Dr.M.P.Purna kishore/Mr.K.Ramakrishna

Subject: Computer Networks (2023-24 SEM II)

Course Outcomes

Subject	CO no	Course outcome	Level	Bloom's Taxonomy(New)
Computer Networks	20CS5T01.1	Illustrate the OSI and TCP/IP reference model	LL2	Comprehension
	20CS5T01.2	Analyze MAC layer protocols and LAN technologies	LL4	Analysis
	20CS5T01.3	Summarize various Routing algorithms and Congestion control principles.	LL2	Comprehension
	20CS5T01.4	Describe Transport layer protocols.	LL2	Comprehension
	20CS5T01.5	Develop application layer protocols	LL3	Applying

CO-PO Mapping & CO-PSO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
20CS5T01.1	3												1		
20CS5T01.2	3	3	3		3								1		
20CS5T01.3			3		3	1	1				1		1		
20CS5T01.4			3		3	1	1				1		1	2	2
20CS5T01.5			3		3	1	1				1	2	1	1	2
	3.00	3.00	2.80		3.00	1.00	1.00				1.00	2.00	1.00	1.33	2.00

* 3-Strong 2-Moderate 1-Slight

Mapping Reasons:

1. CO-1 is completely related to development environment of ComputerNetworks, so CO – 1 strongly map with PO-1.

2. CO-2 is strongly related to Solve problems by using Different LAN Technologies and MAC layer Protocols, so CO-2 strongly maps with PO-1, PO-2, PO-3 and PO-5 and

3. CO-3 is strongly related to Apply Different routing Algorithms, so CO-3 strongly maps with PO-3, PO-5 and weakly maps to PO-6, PO-7 and PO-11.

4. CO-4 is strongly related to Transport Layer Protocols, so CO-4 strongly maps with PO-3, PO-5 and weakly maps to PO-6, PO-7 and PO-11.

5. CO-5 is strongly related to Application Layer Protocols so CO-5 strongly map with PO-3, PO-5 and weakly maps to PO-6, PO-7 and PO-11.

Similarly CO's-PSO's Mapping Reasons:

1. CO-1 is completely related to development environment of Computer Networks, so CO – 1 weakly map with PSO-1.

2. CO-2 is strongly related to Solve problems by using Different LAN Technologies and MAC layer Protocols, so CO-2 weakly maps with PSO-1.

3. CO-3 is strongly related to Apply Different routing Algorithms, so CO-3 weakly maps with PSO-1

4. CO-4 is strongly related to Transport Layer Protocols, so CO-4 weakly maps with PSO-1, and moderately mapped with PSO-2 and PSO-3

5. CO-5 is strongly related to Application Layer Protocols so CO-5 weakly maps with PSO-1, and moderately mapped with PSO-2 and PSO-3

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COs and Mapping with PO/PSO

Name of the Faculty: Mr.K.Ramakrishna
Course: RVSP (20EC5E04)
AY: 2023-24
Class: III B. Tech ECE(1,2&3)
Semester: I

Course Outcomes

After completing this course the student will be able to:

Sl. No.	CO	COURSE OUTCOME	BL
1	C314.1	Understand the basics of probability, events, sample space and how to use them to real life problems.	Understand & Application
2	C314.2	Analyze that the random variable is always a numerical quantity.	Analyze
3	C314.3	Understand the multiple random variables and relate through examples to real problems.	Understand & Application
4	C314.4	Understand the concept of random processes in both deterministic and non deterministic types, & correlation functions.	Understand
5	C314.5	Evaluate the Autocorrelation and its relation with power density spectrum and its properties, Evaluate the autocorrelation function and power spectral density of system response.	Evaluation

Mapping of course outcomes with program outcomes:

High -3 Medium -2 Low-1

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
C314.1	2	3	-	-	-	-	-	-	-	-	-	-
C314.2	2	3	-	-	-	-	-	-	-	-	-	-
C314.3	2	3	-	-	-	-	-	-	-	-	-	-
C314.4	2	3	-	-	-	-	-	-	-	-	-	-
C314.5	2	3	-	-	-	-	-	-	-	-	-	-

Mapping of course outcomes with Performance Indicators:

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
C314.1	1.1.1	2.4.1	-	-	-	-	-	-	-	-	-	-
C314.2	1.1.1	2.4.1	-	-	-	-	-	-	-	-	-	-
C314.3	1.1.1	2.4.1	-	-	-	-	-	-	-	-	-	-
C314.4	1.1.1	2.4.1	-	-	-	-	-	-	-	-	-	-
C314.5	1.1.1	2.4.1	-	-	-	-	-	-	-	-	-	-

Co mapping with PSO

CO/PSO	PSO1	PSO2	PSO3
C314.1	3	-	2
C314.2	3	-	2
C314.3	3	-	2
C314.4	3	-	3
C314.5	3	-	3

CO-PO/PSO mapping Justification:

Mapped POs: PO1, PO2

PO1.	**ENGINEERING KNOWLEDGE:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO2.	**PROBLEM ANALYSIS:** Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PSO1	Able to apply concepts, design, and implement complex systems related to Analog & Digital Circuits, Communications, and Signal Processing.
PSO 3	Able to identify problems in the society and solve by designing projects.

- C314.1. Understand the basics of probability, events, sample space and how to use them to real life problems. **(Understanding & Application)**

	Justification
PO1	Get the knowledge of basics of probability, events, and sample space.
PO2	Find probability of real time events.
PSO1	Able to apply probability concepts in Communications, and Signal Processing.
PSO 3	Able to identify and find probability of real time events in the society

- C314.2. Analyze that the random variable is always a numerical quantity. (Analyzing)

	Justification
PO1	Students acquire knowledge of Random variable.
PO2	Find the mean, variance, skew and skewness and moments of random variable.
PSO1	Able to apply Random variable concepts, design, and implement complex systems related to Analog & Digital Circuits, Communications, and Signal Processing.
PSO 3	Able to identify problems in the society and solve by designing projects.

- C314.3. understand the multiple random variables and relate through examples to real problems. (Understanding & Application)

	Justification
PO1	Get the knowledge of multiple random variables.
PO2	Easily evaluate the expected values of multiple random variables and joint moments
PSO1	Able to apply of multiple random variable concepts, design, and implement complex systems related to Analog & Digital Circuits, Communications, and Signal Processing.
PSO 3	Able to identify problems in the society and solve by designing projects.

- C314.4.Understand the concept of random processes in both deterministic and non deterministic types & correlation functions. (Understanding)

	Justification
PO1	Get the knowledge of random processes and its classification.
PO2	Evaluate the Autocorrelation & Cross correlation functions.
PSO1	Able to apply random processes concepts, design, and implement complex systems related to Analog & Digital Circuits, Communications, and Signal Processing.
PSO 3	Able to identify problems in the society and solve by designing projects.

- C314.5. Evaluate the autocorrelation and its relation with power density spectrum and its properties. (Evaluating)
- Evaluate find the autocorrelation function and power spectral density of system response. (Evaluating)

	Justification
PO1	Get the knowledge of Power spectral density function and its relation with ACF.
PO2	Find ACF from PSD and PSD from ACF.
PSO1	Able to apply Power spectral density concepts, design, and implement complex systems related to Analog & Digital Circuits, Communications, and Signal Processing.
PSO 3	Able to identify problems in the society and solve by designing projects.
PO1	Get the knowledge of LTI system and its Response.
PO2	Find correlation function and power spectral density for LTI System response.
PSO1	Able to apply random processes concepts, design, and implement complex systems related to Analog & Digital Circuits, Communications, and Signal Processing.
PSO 3	Able to identify problems in the society and solve by designing projects.

K. Ravi
Faculty

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DIGITAL SIGNAL PROCESSING

Course Outcomes

Faculty Name: Mrs.K.Sowjanya/Dr.Sarala Patchala **A.Y:** 2023-24

Name of the Course: Digital Signal Processing

Subject Code : 20EC6T02 **Class:** III Year II SEM

CO code	CO Description	Taxonomy Level
C322.1	Apply the difference equations concept in the analysis of Discrete time systems	Understand (TL2)
C322.2	Use the FFT algorithm for solving the DFT of a given signal	Understand (TL2)
C322.3	Design a Digital filter (FIR&IIR) from the given specifications	Apply (TL3)
C322.4	Use the Multirate Processing concepts in various applications (eg: Design of phase shifters, Interfacing of digital systems)	Apply (TL3)
C322.5	Apply the signal processing concepts on DSP Processor.	Apply (TL3)

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DIGITAL SIGNAL PROCESSING

Course Outcomes Mapping with PO's and PSO's

Faculty Name: Mrs.K.Sowjanya/Dr.Sarala Patchala **A.Y:** 2023-24
Name of the Course: Digital Signal Processing
Subject Code : 20EC6T02 **Class:** III Year II SEM

Course Outcomes

CO code	CO Description	Taxonomy Level
C322.1	Apply the difference equations concept in the analysis of Discrete time systems	Understand
C322.2	Use the FFT algorithm for solving the DFT of a given signal	Apply
C322.3	Design a Digital filter (FIR&IIR) from the given specifications	Apply
C322.4	Use the Multirate Processing concepts in various applications (eg: Design of phase shifters, Interfacing of digital systems)	Apply
C322.5	Apply the signal processing concepts on DSP Processor.	Apply

CO-PO Mapping

CO code	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
C322.1	3	2										
C322.2		3	2									
C322.3	1	3	2									
C322.4		3	2									
C322.5		3	2									
Average	2	2.8	2									

CO-PSO Mapping

CO code	PSO1	PSO2	PSO3	PSO4
C322.1	3	2		
C322.2	2	3		
C322.3	2	3		
C322.4	2	3		
C322.5	2	3		
Average	2.2	2.8		

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DIGITAL SIGNAL PROCESSING

CO/PO/PSO JUSTIFICATION

Faculty Name: Mrs.K.Sowjanya/Dr.Sarala Patchala **A.Y:** 2023-24
Name of the Course: Digital Signal Processing
Subject Code : 20EC6T02 **Class:** III Year II SEM

MAPPING	CORRELATION LEVELS	MAPPING REASONS
C322.1-PO1	3	Classify and analyze discrete time signals and systems
C322.1-PO2	2	Find the response of system in time domain.
C322.1-PSO1	3	Apply & analyze various system Response through Z-Transform.
C322.1-PSO2	2	Implementation of various discrete signal generation in MATLAB
C322.2-PO2	3	For DFT computation, students should have the basic knowledge of solving complex numbers
C322.2-PO3	1	Implementation of DFT& FFT Algorithms in MATLAB
C322.2-PSO2	3	Discrete Fourier Transform concepts could help in identifying the feasibility of the system
C322.2-PSO1	2	Provide an idea for design solutions in complex frequency domain
C322.3-PO2	3	Integration concepts to be used for designing filters
C322.3-PO3	2	Recognize the applications of IIR Filter design in science and engineering
C322.3-PO1	1	Identify the applications of FIR Filter design in science and engineering
C322.3-PSO2	3	Obtain appropriate understanding about the stable filter design
C322.3-PSO1	2	Apply FIR Filter design for processing signals using MATLAB
C322.4-PO2	3	Implementation of Multi-Rate Signal Processing Techniques
C322.4-PO3	2	Analyze the effect of multi rate in different applications
C322.4-PSO2	3	Employ MATLAB tool to interpret basics of Multi-Rate Signal processing.
C322.4-PSO1	2	Identify various real-time applications of Multi-rate Signal Processing
C322.5-PO2	3	Architecture of dsp processor and instruction set, addressing modes in detail compare with microcontrollers
C322.5-PO3	2	Implementation of DSP processors in real time projects
C322.5-PSO2	3	Identify various real-time applications on DSP processors
C322.5-PSO1	2	Obtain appropriate understanding about the processor interfacing design using MATLAB/cc studio

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Department of Electronics and Communication Engineering

LESSON PLAN

Name: Dr.Sk.Sadulla/Dr.A.Sarath Kumar **Class: III B. Tech II SEM (R-20)**

Subject: VLSI DESIGN **Branch: ECE** **A.Y:2024-25**

S.No	Name of the topic	Method	Reference (Page number)
	UNIT- I: INTRODUCTION AND BASIC ELECTRICAL PROPERTIES OF MOS CIRCUITS		
Lecture-1	Introduction to IC technology	GB & CP	T1:1-4
Lecture-2	Fabrication process: nMOS, pMOS and CMOS	GB & CP	T1:9-20
Lecture-3	Ids versus Vds Relationships	GB & CP	T1:25-28
Lecture-4	Aspects of MOS transistor Threshold Voltage	GB & CP	T1:28
Lecture-5	MOS transistor Transconductance	GB & CP	T1:31
Lecture-6	Output Conductance and Figure of Merit	GB & CP	T1:31
Lecture-7	nMOS Inverter	GB & CP	T1:34
Lecture-8	Pull-up to Pull-down Ratio for nMOS inverter driven by another nMOS inverter	GB & CP	T1:36
Lecture-9	and through one or more pass transistors, Alternative forms of pull-up	GB & CP	T1:37
Lecture-10	The CMOS Inverter, Latch-up in CMOS circuits	GB & CP	T1:43-45
Lecture-11	Bi-CMOS Inverter, Comparison between CMOS and BiCMOS technology	GB & CP	T1:48-53
UNIT-II: OVERVIEW OF VLSI DESIGN METHODOLOGY and STICK DIAGRAM AND LAYOUT DESIGN RULES			
Lecture-12	VLSI Design Flow,	PPT Presentation	W1
Lecture-13	Architectural design, Logical design	PPT Presentation	W1
Lecture -14	Physical design	PPT Presentation	W1
Lecture -15	MOS Layers, Stick Diagrams	GB &CP	T1:55-56
Lecture-16	Design Rules and Layout	GB &CP	T1:66-72
Lecture-17	Layout Diagrams for MOS circuits	GB &CP	T1:65-76
UNIT-III: BASIC CIRCUIT CONCEPTS and SCALING OF MOS CIRCUITS			
Lecture-18	Sheet Resistance, Sheet Resistance concept applied to MOS transistors and Inverters	GB &CP	T1:86-87
Lecture-19	Area Capacitance of Layers	GB &CP	T1:89
Lecture-20	Standard unit of capacitance	GB &CP	T1:90
Lecture-21	some area Capacitance Calculations	GB &CP	T1:91

Lecture-22	The Delay Unit, Inverter Delays	GB & CP	T1:93-94
Lecture-23	driving large capacitive loads, Propagation Delays	GB & CP	T1:98-104
Lecture-24	Wiring Capacitances, Choice of layers.	GB & CP	T1:106-110
Lecture-25	SCALING OF MOS CIRCUITS: Scaling models and scaling factors	GB & CP	T1:114
Lecture-26	Scaling factors for device parameters	GB & CP	T1:115
Lecture-27	Limitations of scaling, Limits due to sub threshold currents	GB & CP	T1:121-126
Lecture-28	Limits on logic levels and supply voltage due to noise and current density	GB & CP	T1:128
	UNIT-IV: CMOS STATIC AND DYNAMIC CIRCUIT DESIGN		
Lecture-29	**CMOS Static and Dynamic Circuit Design**	GB & CP	T1:220
Lecture-30	Compelmentry CMOS,Rationed Logic	GB & CP	W2
Lecture-31	Rationed Logic, Pass-Transistor Logic	GB & CP	T1:136
Lecture-32	**Dynamic CMOSDesign**		
Lecture-33	Dynamic logic basic principles	GB & CP	T1:166
Lecture-34	Speed and Power Dissipation of Dynamic Logic	GB & CP	T1:167
Lecture-35	Issues in Dynamic Design	GB & CP	T1:169
Lecture-36	Cascading Dynamic Gates, Choosing a Logic Style		T1:171
Lecture-37	Gate Design in the Ultra Deep-Submicron Era	GB & CP	
Lecture-38	Latch Versus Register, Latch based design	GB & CP	T1:310
Lecture-39	timing decimation, positive feedback	GB & CP	T1:172
Lecture-40	instability,Metastability	GB & CP	T1:172
Lecture-41	multiplexerbased latches	GB & CP	T1:173
Lecture-42	Master-Slave Based Edge Triggered Register	GB & CP	T1:175
Lecture-43	clock to q delay, setup time, hold time	GB & CP	T1:176
Lecture-44	reduced clock load master slave registers,	GB & CP	T1:177
Lecture-45	Clocked CMOSregister.	GB & CP	T1:178
Lecture-46	Cross coupled NAND and NOR	GB & CP	T1:180
Lecture-47	SR Master Slave register	GB & CP	T1:182
Lecture-48	Storage mechanism, pipelining	GB & CP	T1:182
	UNIT-V: FPGA DESIGN and INTRODUCTION TO ADVANCED TECHNOLOGIES		
Lecture-49	FPGA DESIGN:	GB & CP	R3:10
Lecture-50	FPGA design flow	GB & CP	R3:12
Lecture-51	Basic FPGA architecture	Online lecture	R3:13
Lecture-52	FPGA Technologies	GB & CP	R3:15
Lecture-53	Introduction to FPGA Families	GB & CP	R3:16
Lecture-54	INTRODUCTION TO ADVANCED TECHNOLOGIES	Online lecture	R3:18

Lecture-55	Giga-scale dilemma	GB & CP	R3:19
Lecture-56	Short channel effects,	GB & CP	R3:20
Lecture-57	High–k	Online lecture	R3:21
Lecture-58	Metal Gate Technology	GB & CP	R3:23
Lecture-59	FinFET	Online lecture	R3:25
Lecture-60	TFET.	GB & CP	R3:25

Google classroom is used as LMS for the entire course

TEXT BOOKS:

T1: Essentials of VLSI Circuits and Systems - Kamran Eshraghian, Douglas and A. Pucknell And SholehEshraghian, Prentice-Hall of India Private Limited, 2005 Edition.

T2: Design of Analog CMOS Integrated Circuits by BehzadRazavi , McGraw Hill, 2003

T3: Digital Integrated Circuits, Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic,2nd edition,2016.

REFERENCE BOOKS:

R1: "Introduction to VLSI Circuits and Systems", John P. Uyemura, John Wiley & Sons, reprint 2009.

R2: Integrated Nanoelectronics: Nanoscale CMOS, Post-CMOS and Allied Nanotechnologies Vinod Kumar Khanna, Springer India, 1st edition, 2016.

R3: FinFETs and other multi-gate transistors, ColingeJP, Editor New York, Springer,2008

Web REFERENCES

W1: https://www.geeksforgeeks.org/vlsi-design-cycle/

W2: http://www.mmmut.ac.in/News_content/10305tpnews_05142020.pdf

1)

2)

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